DEFECT DESIGN OF INSULATION SYSTEMS FOR PHOTOVOLTAIC MODULES*

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ABSTRACT

A defect-design approach to sizing electrical insulation systems for terrestrial photovoltaic modules is presented. It consists of gathering voltage-breakdown statistics on various thicknesses of candidate insulation films whence, for a designated voltage, module failure probabilities for enumerated thickness and number-of-layer film combinations are calculated. Cost analysis then selects the most economical insulation system. A manufacturing yield problem is solved to exemplify the technique. Results for unaged Mylar suggest using fewer layers of thicker films.

Defect design incorporates effects of flaws in optimal insulation system selection, and obviates choosing, a priori, a tolerable failure rate--the optimization process does that. Exposure to weathering and voltage stress reduces the voltage-withstanding capability of module insulation films. Defect design, applied to aged polyester films, promises to yield reliable, cost-optimal insulation systems.

INTRODUCTION

The goals of the Jet Propulsion Laboratory's Low-Cost Solar Array Project are to establish, by 1986, an industrial capability of manufacturing terrestrial photovoltaic modules at an f.o.b. price of \$0.70/watt or \$70/m^2 in 1980 dollars (1). Of this cost goal, \$14/m^2 is allocated for encapsulation and insulation materials, one function of which is to provide the electrical isolation necessary for safe and reliable performance. Present performance and reliability goals include a nominal 20-year module service life with a field failure rate not exceeding a projected five modules per thousand per year.

This paper presents results of a program whose objective is to determine methods of designing flatplate photovoltaic module electrical insulation systems consistent with the cost and performance goals cited above.

Defects

From an electrical viewpoint, a photovoltaic module consists of electrically active, interconnected solar cells encapsulated in a material that isolates the active elements from the module frame and/or metal substrate (Figure 1). With a glass superstrate providing structural strength, a metal substrate may be replaced by a foil, i.e., a metallized polyester film.

The module electrical isolation design problem is inherently statistical, since random material and manufacturing defects will essentially govern, for each module at its operating voltage in the array, the time at which electrical break-down may occur or, during hi-pot testing, the voltage at which breakdown may occur.

Typical defects that increase the likelihood of electrical insulation failure include (see Figure 1):

(1) Local stress intensification sites on electrified parts, such as sharp edges and corners on cells and conductors, and jagged projections likely to occur at solder sites and along the cell metallization.

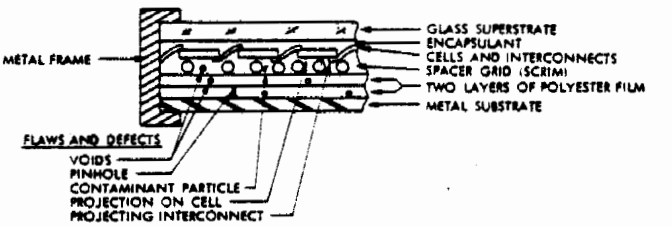

Figure 1. Elements of PV Module Construction and Some Typical Manufacturing Defects

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(2) Voids, pinholes, and contaminant particles in the insulating materials.

Module design and manufacturing procedures must account for defects, either by minimizing their number, e.g., clean-room manufacturing standards and effective quality control, and/or by minimizing their deleterious effects; e.g., using thick layers of insulation to ensure low voltage stress, or breakdown-resistant materials (2). Cost-tradeoff analyses will establish the extent to which any or all of these or other strategies should be employed.

Electrical Breakdown of Solid Insulation

Several breakdown mechanisms have been identified (3). These include:

(1) Intrinsic (electronic) breakdown: electron-induced formation of a conductive path through the insulation. Voltage-stress levels are very high and the breakdown event occurs over tens of nanoseconds.

(2) Electromechanical breakdown. The very high applied voltage stress compresses the material, resulting in electronic breakdown at less than intrinsic strength levels. The compression effect becomes more pronounced at higher temperatures and is attributed to a reduction of Young's modulus with increasing temperature.

(3) Divergent field breakdown. Local stress enhancement at sharp conductive points in contact with the insulation, or conductive particle inclusions within the insulation itself, even at relatively low applied voltages, may be sufficient to induce intrinsic or electromechanical breakdown, depending upon the temperature.

(4) Internal discharge breakdown (partial discharge, corona). Gas-filled cavities (voids) within the insulation serve as stress enhancement sites. Low-energy discharges occur frequently, even at relatively low operating voltages, and gradually, but with increasing rapidity, erode the insulation material. The erosion is chemical (depolymerization) and/or thermal (carbonization) in nature. Eventually, fine conductive channels (trees) propagate throughout the material, causing failure. The process can take many years.

(5) Surface discharge breakdown. Arcs from electrode edges impinging on an adjacent dielectric surface can induce erosion by ionic bombardment, chemical degradation, and heating, leading ultimately to failure. Carbonized conducting paths (tracks) on or just below the surface of the material is a signature of this breakdown process.

The first two breakdown processes are now recognized as defect-independent properties of the insulation material; some representative intrinsic breakdown stresses of candidate insulation materials, taken from the general literature, are presented in Table 1.

Table 1. Intrinsic Voltage Breakdown Stresses and Computed Minimum Thicknesses of Insulations

Material	Intrinsic Stress E_{BD} (kV/mil)	Minimum Thickness $t = \frac{V}{E_{BD}}$ (mil) $V = 1.80$ kV	$V = 5.80$ kV
Silicone Rubber	0.75	2.40	7.73
PVB	0.35	5.14	16.57
Mylar	7.50	0.24	0.77
EPR	0.50	3.60	11.60
EVA	0.62	2.90	9.35
Tedlar	3.50	0.51	1.66
Polyethylene	0.50	3.60	11.60

The latter three breakdown processes are flaw- or defect-dependent and are of major concern to the photovoltaic module designer. Flaws associated with the cell string enhance the likelihood of divergent field breakdown and are treated in the next section. Flaws associated with the insulation materials enhance the likelihood of internal discharge breakdown and are treated in a subsequent section. Surface discharge breakdown at module electrical terminations is not treated in this paper, although surface discharge phenomena are accounted for in breakdown testing. Results, suggestions, and conclusions are presented in the final section.

FLAWS ASSOCIATED WITH THE CELL STRING (ELECTRODE)

Cell-string flaws are classified as follows:

(1) Sharp points and edges, which concentrate the local field strength.

(2) Offsets and projections, such as the soldered interconnect on the underside of a cell, which reduce the cell-to-ground distance d, thereby increasing the local voltage stress.

Analytical and Theoretical Considerations

Sharp Points. Mason (3) gives formulas for computing stress enhancement factors at the tip of sharp conductive hyperboloidal points:

$$\sigma = \frac{E_{max}}{E_{AV}} = \frac{2\ pd}{\ln q}$$

where

$$pd = \sqrt{\frac{d}{r}\left(1 + \frac{d}{r}\right)}$$

$$q = 1 + 2\left(\frac{d}{r} + pd\right)$$

d = point-to-plane distance

r = radius of conductive point

$E_{AV} = \frac{V}{d}$, where V is the applied voltage

For clarity in subsequent analysis, Mason's equation is replotted in Figure 2 as a family of upward-sloping curves with point radius r as parameter. Note that increasing the gap separation at constant voltage and point radii increases the stress enhancement factor, perhaps contrary to intuition. But calculations reveal that the local field strength actually decreases because the decrease of the average field more than compensates for the increased stress concentration. Also noteworthy is the observation that increasing the point radii at constant voltage and gap separation correspondingly reduces the stress enhancement factor and the local field strength. These two observations suggest the use of spacers to maintain adequate separation between solar cells and ground, and also suggest that the surfaces of solar cells be lightly polished to blunt sharp radii, assuming that is feasible.

Offsets and Projections. Also plotted in Figure 2 are downward-sloping curves that depict the influence of projections, which is observed to be small unless a projection is more than half the size of the gap. This too suggests the use of spacers and care in soldering interconnects to cells.

The latter curves are obtained from uniform field air-gap voltage breakdown data (4), which is given approximately as $V = 0.16d^{0.9}$, by plotting the ratio of the breakdown voltage for a gap d without an offset to that for a gap d with an offset d' vs the gap separation d, i.e.,

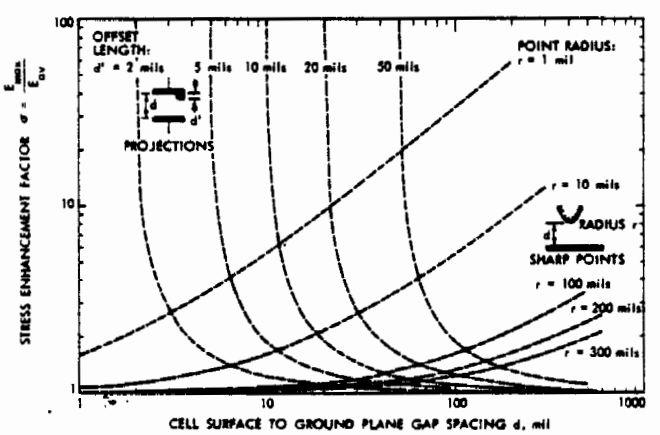

Figure 2. Stress Enhancement Due to Sharp Points and Projections

$$\sigma = \frac{V}{V'} = \frac{0.16d^{0.9}}{0.16(d - d')^{0.9}} = \left(\frac{d}{d - d'}\right)^{0.9} \qquad (1)$$

In these equations, V and V' are in kilovolts and d and d' are in mils.

Experimental Data

In an effort to understand the effects of sharp edges and other stress-intensifying flaws on electrified parts of modules, paired cells from several manufacturers were interconnected and electrified until breakdown of the measured air gap between the cells and a copper ground plate resulted. Cell-sized brass discs with lightly polished surfaces and smoothed edges were similarly tested. The apparatus is shown in Figure 3 and the data are presented in Figure 4. The data plots (solid curves) in Figure 4 are obtained by dividing the measured gap breakdown voltage by the uniform field breakdown voltage (see above) for the same gap length and plotting against the gap length. These curves are superposed on the theoretical curves of Figure 2. It is immediately evident that, at large air gaps, point-to-plane effects (probably arising from the sharp (90°) edge) dominate breakdown behavior, while at small gaps, offset and projection effects dominate. It is the latter that will dominate cell discharge behavior in photovoltaic modules.

Design Considerations

The results of the previous sub-sections suggest, since cell-string projections—particularly the offset resulting from interconnect attachment—govern cell-string discharge behavior, that spacers (scrims) be used to provide the necessary gap

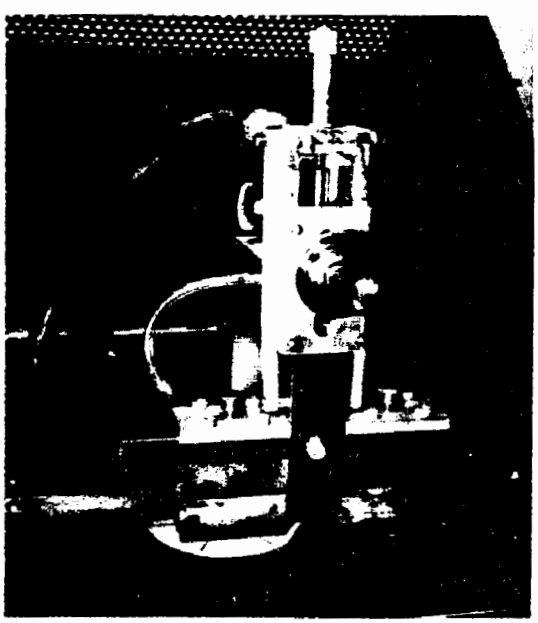

Figure 3. Cell-String Flaw Characterization Apparatus

separation. The data of Figure 4 indicate that an air gap greater than 60-mils may be required. However, the breakdown mechanisms in dielectric solids differ considerably from those in air, so these data are not directly applicable to solar cells encapsulated in a module, other than to indicate trends. A dielectric will reduce geometric cell-string stress-enhancement factors by a factor equal to the dielectric constant. In the case of Mylar or EVA ($\epsilon \approx 3.2$) this reduction is by more than a factor of 3. A cell-to-ground separation of at least 20 mils is recommended for encapsulated cells, based upon these considerations.

Another technique for sizing polyester film insulation for modules involves using a safety factor with thicknesses calculated from intrinsic or short-time dielectric stress data (5). Based upon this approach, the Insulated Power Cable Engineers Association (IPCEA) recommends for ac cable insulation design a maximum design stress at only 0.5% of the intrinsic stress, and for dc a maximum design stress at 1.5% of the intrinsic stress (5). This corresponds to a safety factor of 67 for use with the thicknesses calculated in Table 1. Based upon that reasoning, up to 16 mils of Mylar at 1800 V, and up to 52 mils at 5800 V, is indicated. These voltages represent typical hi-pot test voltages for residential (250-V) and central-station (1500-V) applications (Figure 5).

FLAWS ASSOCIATED WITH INSULATION (DIELECTRIC)

The flaws associated with thin-film dielectrics include pinholes, gas inclusions (voids), and embedded particles.

Analytical and Theoretical Considerations

Paschen's curve, Figure 6, quantifies the discharge behavior of air gaps under uniform field conditions. A voltage as low as 327 V will initiate breakdown in a 0.28-mil-deep air gap. If the air gap is embedded in a dielectric medium in the

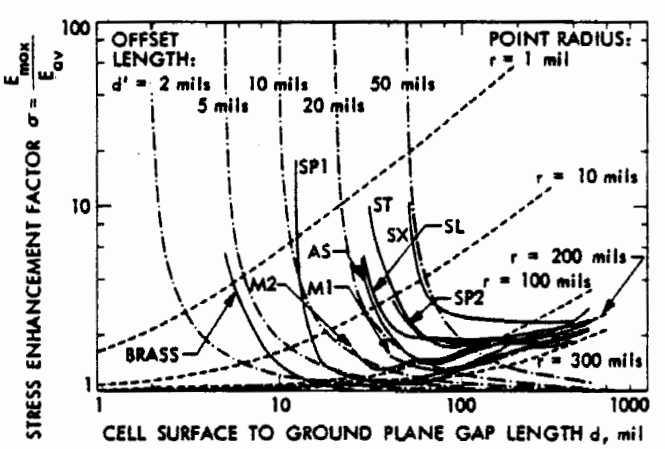

Figure 4. Cell-String Data Superposed on Theoretical Curves, Depicting Effects of Sharp Points and Projections

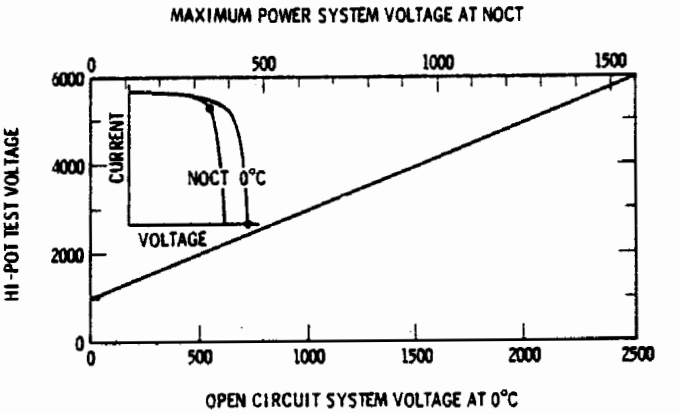

Figure 5. Module Dielectric Test Voltages (7)

form of a void, its discharge behavior is altered: the minimum applied voltage at which the void discharges is given for ac as

$$V = E_a \left[t_a + \frac{1}{\epsilon_d}\left(t_d - t_a\right)\right] \qquad (2)$$

and for dc as

$$V = E_a \left[t_a + \frac{\rho_d}{\rho_a}\left(t_d - t_a\right)\right] \qquad (3)$$

where

E_a = breakdown voltage stress of air void of depth t_a (from Paschen's curve, Figure 6)

t_d = thickness of dielectric

ϵ_d = dielectric constant of insulation

ρ_d, ρ_a = volume resistivities of dielectric and air void, respectively

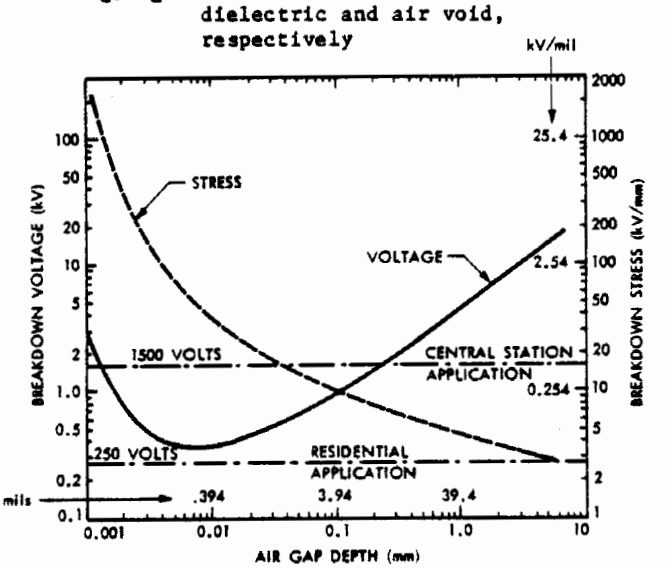

Figure 6. Paschen's Curve for Air Gaps at Atmospheric Pressure

These formulas apply as well to the breakdown of an air gap between the curved edges of a test electrode and an adjacent dielectric surface (6).

Residential modules, in operation at voltages below the Paschen minimum, are not expected to suffer internal discharge breakdown, but central-station modules operate well above internal discharge starting voltages, and modules with defects may fail quickly in such an applications environment.

The basic test of an insulation's electrical isolation capability is the hi-pot test, which module manufacturers conduct as a routine part of acceptance testing. The hi-pot test is a one-minute application of more than twice operating voltage plus 1000 V between the cell string and the grounded frame (Figure 5) (7). Practically, a module insulation system must be designed to pass the hi-pot test.

Experimental Data

In order to quantify module insulation breakdown probability vs applied voltage, breakdown testing was conducted on large areas of single-layer polyester films. The film breakdown test apparatus is shown in Figure 7. The electrodes are 1-in.-dia, flat-ended (plane-to-plane) brass cylinders with 3/32-in. rounded edges. The rate of voltage rise was 500 V/sec. All tests were conducted in air at atmospheric pressure. The bulk of the breakdowns observed occurred within the projected electrode area, although as sample thicknesses increased, surface discharge breakdowns became more frequent. The effective electrode area was considered as extending beyond the projected electrode area to the edge of the corona ring (6). For residential applications, maximum power system voltage at NOCT is taken as 250 V. From Figure 5, the hi-pot test voltage is about 1800 V. For central-station applications the system voltage is taken as 1500 V, and the hi-pot test voltage is about 5800 V. Using these voltages in Equation (2) permits the calculation of the effective electrode area. These are 0.63 in.^{2} at 1800 V and 0.76 in.^{2} at 5800 V. For simplicity, the test area is taken as 0.75 in.^{2}.

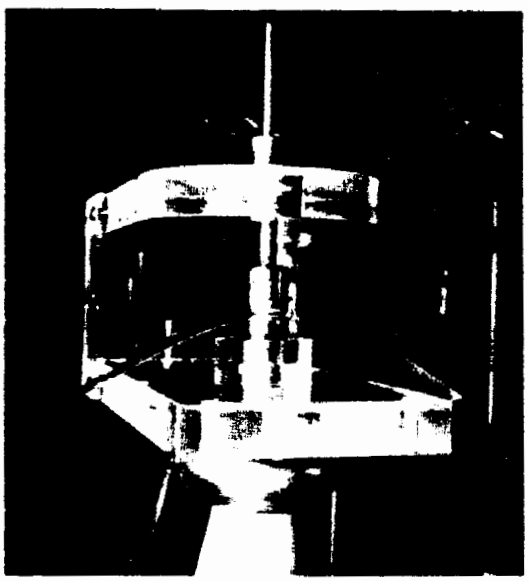

Figure 7. High-Voltage Test Electrodes for Thin-Film Breakdown Experiment

The voltage-probability data for Mylar and Tedlar appear in Figure 8. It is of interest to note that the Tedlar films generally exhibited better performance than the Mylar in the sense that lower breakdown probabilities were obtained for the same applied voltages, despite the fact that Tedlar has a lower dielectic strength than Mylar (Table 1). This is explained by considering the plots of volume flaw density vs applied voltage stress (Figure 9). It is observed that the three Tedlar curves exhibit essentially the same flaw distribution. The Mylar curves exhibit wide variations with thickness but, except for the 3-mil Mylar, this material contains significantly more flaws sensitive to low-voltage stresses than does Tedlar. The technique of generating flaw density vs voltage stress plots uses statistical procedures from brittle fracture analysis (8,9) and is not explained here.

Design Techniques

In a previous section a design technique was considered for sizing insulation film thicknesses based upon cell-string flaw data and intrinsic breakdown stress data. That approach requires the selection of a safety factor that, at best, can be quite arbitrary. Too large a factor may result in an excessive material-cost penalty; too small a factor may result in large module field replacement

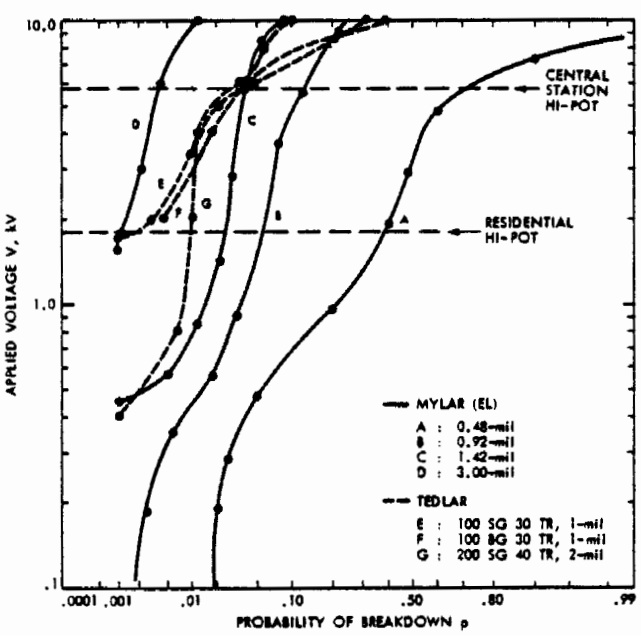

Figure 8. Breakdown Voltage V vs Probability p of Failure of Mylar & Tedlar (Experimental)

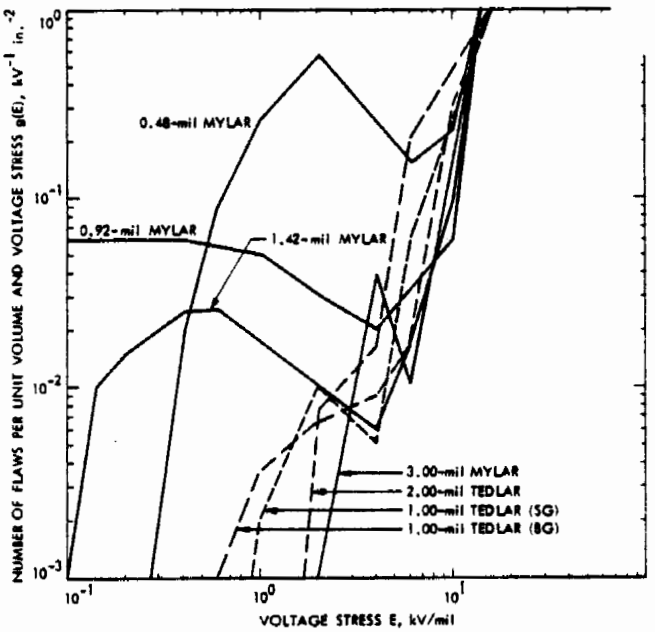

Figure 9. Volume Flaw Density vs Voltage Stress in Mylar and Tedlar

costs. A cost trade-off analysis may effectively be employed to select the appropriate safety factor.

Another design approach seeks to size insulation films so that the applied voltage is below that required to induce internal discharges in voids. The appropriate tools are Paschen's curve and Equations (2) or (3). For an assumed void depth—a major drawback of this method—a stress value is obtained from Paschen's curve. Using this and Equation (2) with Mylar ($\epsilon = 3.2$) and assuming that $t_a = 0.28$ mil, it is found that $t_d = 3.92$ mil at $V = 1800$ V. The ac equation, Equation (2), is used because ϵ is a more stable quantity than ρ and it is more appropriate for hi-pot voltage-test environments.

A preferred design technique is based upon using the voltage breakdown statistics obtained from measurements on candidate insulation systems together with a costing analysis.

If polyester films are to be considered for module insulation systems, it is logical to suppose that such systems will consist either of one thick sheet or of a layered composite of several thin sheets; both strategies reduce the effects of flaws. In either case, the probability p_F of module failure is

$$p_F = 1 - (1 - p^m)^n \qquad (4)$$

where

p = probability that a small test area ($A = 0.75\text{-in}^2$) contains a breakdown-causing defect

m = number of film layers

n = number of test areas per module

$A = 2 \times 4$ ft, $n = 1536$
$A = 4 \times 4$ ft, $n = 3072$
$A = 4 \times 8$ ft, $n = 6144$

The probability p is voltage-dependent and must be measured for each candidate insulation film (Figure 8).

The module manufacturer's concern is that his modules pass the acceptance and qualification tests, in particular the hi-pot test. The manufacturer will increase his module price to the customer to reflect the cost of producing those modules that fail this test. The economic situation is a manufacturing yield problem for which the cost of manufacturing a single module, in $\$/m^2$, is

$$C_M = 88 + mtC_I + (m - 1)tC_L \qquad (5)$$

where

88 = module cost less dielectric, $\$/m^2$, based upon 12.5% efficiency and \$0.70/W market price

m = number of layers

t = film thickness, mils

C_I = cost of film, $\$/m^2$/mil

C_L = cost of layering, $\$/m^2$/mil

The charge to the customer for marketable modules is

$$C_T = \frac{1}{1 - p_F} C_M \qquad (6)$$

Clearly the market price represents a trade-off between manufacturing costs and module rejection (yield).

Cost parameters necessary for the analysis are presented in Table 2 in a format directly applicable for use in Equations (4) to (6). The results are shown in Table 3.

These results indicate that, based upon specimen thicknesses available for measurement, a 2 x 4-ft module with two layers of 3-mil Mylar achieves the minimum cost at both hi-pot test levels. These optimal modules are identical in

Table 2. Parameters Used in Cost Analysis

Module Manufacturing Costs				
Thickness t, mils	0.48	0.92	1.42	3.00
C_I, $\$/m^2$/mil	0.206	0.196	0.195	0.188
C_L, $\$/m^2$/mil	2.92m - 2.69	2.34m - 2.93	1.74m - 1.59	1.22m - 1.00

Table 3a. Results of Manufacturing Yield Cost Analysis for Mylar Film Insulation Systems

2 x 4-ft Module

V_{hi-pot} = 1800 V				V_{hi-pot} = 5800 V			
t mil	m	P_F	C_T $\$/m^2$	t mil	m	P_F	C_T $\$/m^2$
0.48	9	.248	238.58	0.48	26	.259	1307
	10	.104	226.95		27	.194	1290
	11	.041	240.05		28	.144	1301
0.92	3	.248	127.68	0.92	4	.355	165.11
	4	.016	108.21		5	.055	128.29
	5	.001	121.29		6	.007	141.23
1.42	2	.587	221.56	1.42	2	.891	839.81
	3	.021	101.30		3	.081	107.90
	4	.001	112.12		4	.003	112.42
3.00	1	.842	560.07	3.00	1	.997	∞
	2	.002	93.65		2	.021	95.43
	3	0.00	105.65		3	0.00	105.66

construction; the higher cost of the high-voltage module merely reflects the order-of-magnitude-larger failure probability at the higher hi-pot test voltage. Modules that fail the 5800-V hi-pot test but subsequently pass the 1800-V test can be marketed as low-voltage modules.

Table 3b. Results of Manufacturing Yield Cost Analysis for Mylar Film Insulation Systems

4 x 4-ft Module

V_{hi-pot} = 1800 V				V_{hi-pot} = 5800 V			
t mil	m	P_F	C_T $\$/m^2$	t mil	m	P_F	C_T $\$/m^2$
0.48	9	.435	317.38	0.48	28	.267	1520
	10	.197	143.67		29	.201	1490
	11	.081	250.43		30	.149	1494
0.92	3	.434	169.69	0.92	4	.584	256.05
	4	.032	109.98		5	.108	135.81
	5	.002	121.40		6	.015	142.28
1.42	2	.830	535.69	1.42	3	.155	117.39
	3	.042	103.48		4	.006	112.78
	4	.001	112.17		5	.0002	129.93
3.00	1	.975	3541	3.00	1	1.00	∞
	2	.004	93.86		2	.041	97.46
	3	0.00	105.65		3	.0002	105.67

Table 3c. Results of Manufacturing Yield Cost Analysis for Mylar Film Insulation Systems

4 x 8-ft Module

V_{hi-pot} = 1800 V				V_{hi-pot} = 5800 V			
t mil	m	P_F	C_T $\$/m^2$	t mil	m	P_F	C_T $\$/m^2$
0.48	10	.356	315.57	0.48	31	.207	1708
	11	.156	272.55		32	.154	1701
	12	.063	277.21		33	.113	1723
0.92	3	.680	299.74	0.92	5	.204	152.22
	4	.063	113.60		6	.029	144.41
	5	.004	121.62		7	.004	164.14
1.42	2	.971	3147	1.42	3	.286	138.94
	3	.081	107.96		4	.013	113.50
	4	.002	112.28		5	.0005	129.96
3.00	1	.999	∞	3.00	1	1.00	∞
	2	.009	94.28		2	.081	101.65
	3	0.00	105.65		3	.0003	105.68

Generally, the analysis suggests the use of fewer layers of thicker films and that optimal costs are insensitive to module size.

SUMMARY AND CONCLUSIONS

It has been shown that the electrical isolation problem in the design of module insulation systems requires a consideration of flaws and defects, both on the cell string and in the insulation itself. Defect design provides favorable cost economics while satisfying desired reliability criteria. The cost analysis yields the module failure probability and suggests the use of fewer layers of thicker films. Optimal costs are insensitive to module size.

A review of the effects of cell-string defects suggests the use of an inexpensive bulk pottant, high-dielectric films, and scrim spacers.

A manufacturing yield problem has been solved, based upon satisfying routine acceptance (hi-pot) test requirements. A correlation between field failure probability and hi-pot failure probability is not presently known to exist. Establishing such a correlation, if possible, will be a major contribution to the photovoltaic industry.

Field failure probability (as opposed to hi-pot failure probability) is more likely governed by the voltage endurance of the insulation materials used. The methods of this paper can be applied to that problem by gathering breakdown data on aged insulation films and conducting a least-life-cycle costing analysis (10, 11). This work is presently in progress at JPL.

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REFERENCES

1. Aster, R.W., "Price Allocation Guidelines January 1980," JPL Publication 80-51, January 1980.

2. Mason, J.H., "Discharges," IEEE Trans. Elec. Insul., V. EI-13, No. 4, pp. 211-238, 1978.

3. Mason, J.H., "Dielectric Breakdown in Solid Insulation," Progress in Dielectrics, V. 1, pp. 1-58, 1959.

4. Reference Data for Radio Engineers, ITT, 4th Edition.

5. "Study of Curved Glass Photovoltaic Module and Module Electrical Isolation Design Requirements," Bechtel National, Inc., DOE/JPL - No. 954698-80/2, Final Report, June 1980.

6. Halleck, M.C., "Calculation of Corona-Starting Voltage in Air-Solid Dielectric Systems," Trans. A.I.E.E., V. 75, pp. 211-216, 1956.

7. "Flat-Plate Photovoltaic Module and Array Circuit Design Optimization," Jet Propulsion Laboratory, 1980 (Proceedings of Workshop, May 19 and 20, 1980).

8. Matthews, J.R., McClintock, F.A., and Shack, W.J., "Statistical Determination of Surface Flaw Density in Brittle Materials," J. Amer. Ceram. Soc., V. 59 (7-8), pp. 304-308, 1976.

9. Evans, A.G., and Jones, R.L., "Evaluation of a Fundamental Approach for the Statistical Analysis of Fracture," J. Amer. Ceram. Soc., V. 61 (3-4), pp. 156-160, 1978.

10. Ross, R.G., Jr., "Flat-Plate Photovoltaic Array Design Optimization," 14th IEEE Photovoltaic Specialists Conference, pp. 1126-1132, 1980.

11. Ross, R.G., Jr., "Photovoltaic Design Optimization for Terrestrial Applications," 13th IEEE Photovoltaic Specialists Conference, pp. 1067-1073, 1978.