DEVELOPMENT OF DESIGN CRITERIA AND QUALIFICATION TESTS FOR BYPASS DIODES IN PHOTOVOLTAIC APPLICATIONS

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ABSTRACT

The Flat-Plate Solar Array (FSA) Project at the Jet Propulsion Laboratory (JPL) includes a research program directed at improving photovoltaic (PV) module and array reliability. One aspect of this program addresses the development of a method for assessing the design adequacy and relative long-term reliability of bypass diodes.

PV designers use bypass diodes to limit the detrimental effects of array shadowing and internal open-circuit module failures, and thereby to maximize the system's energy output during its operational life. An important consideration is the long-term reliability of the diodes and the factors controlling their junction temperature. These include derating of the diode characteristics, adequacy of the heat-sink design and the expected worst-case thermal environment for PV applications.

Presented are specific design criteria for the maximum allowable, and long-life allowable, values of junction temperatures of p-n and Schottky bypass diodes, and a test method for assessing conformance to the design criteria. Junction temperatures are defined in terms of expected worst-case field conditions, including ambient temperature and solar irradiance impinging on the PV module. The rating criteria therefore address the maximum allowable current and heat-sink adequacy for diodes mounted integral with or external to module assemblies. The method establishes worst-case module-to-diode thermal interfaces and is adaptable for laboratory or field-site junction-temperature assessments using standard relationships convenient to the PV designer. The design criteria and test method presented should be useful in establishing a cost-effective qualification test to assess diode reliability, in configuring heat sinks and in selecting reliable diodes.

Key Words: Photovoltaic, Bypass Diode, Design Criteria, Qualification Test

I. INTRODUCTION

Bypass Diodes: Photovoltaic Applications

The location and method of installation of bypass diodes in photovoltaic modules and arrays varies with manufacturer and user requirements; common configurations are described in Figure 1. Single or multiple diodes may be integral with the module, either embedded within the laminate assembly adjacent to solar cells, or installed in the electrical junction box on the module's back surface as in Figure 1a and 1b. Diodes within the junction box may be mounted across the terminal posts, on p-c boards, brackets or even embedded in a junction box pottant. A single diode may also be mounted on the array support structure or wiring harnesses that are considered external to the module or panel assemblies (series-connected or parallel-connected module groups) as in Figure 1c, 1d, and 1e. In these cases, diodes are not in intimate contact with the module or panel environment, but are nearby and receive thermal input from these sources by radiation.

Unlike conventional power-rectifying diodes, bypass diodes in PV circuits have operating stresses characterized by two functional modes. When the solar cell group is operating normally, the diodes are reverse-biased, blocking current. This operating mode, characterized by prolonged operation at a relatively low reverse voltage (typically 6 to 12 V) during daylight hours and with no voltage stress at night, has been examined in detail by Shepard.[1,2,3] The low junction temperature (45°C to 60°C) and low level of reverse voltage

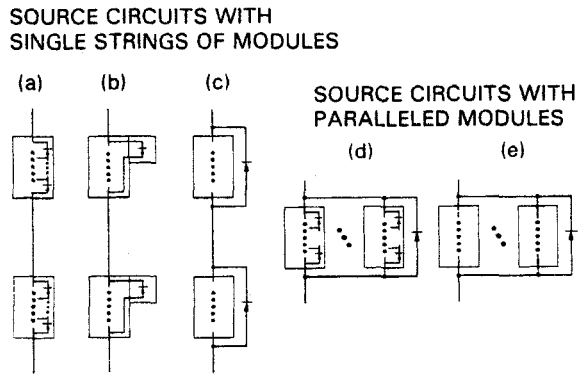

Figure 1. Bypass diode locations in photovoltaic modules and arrays.

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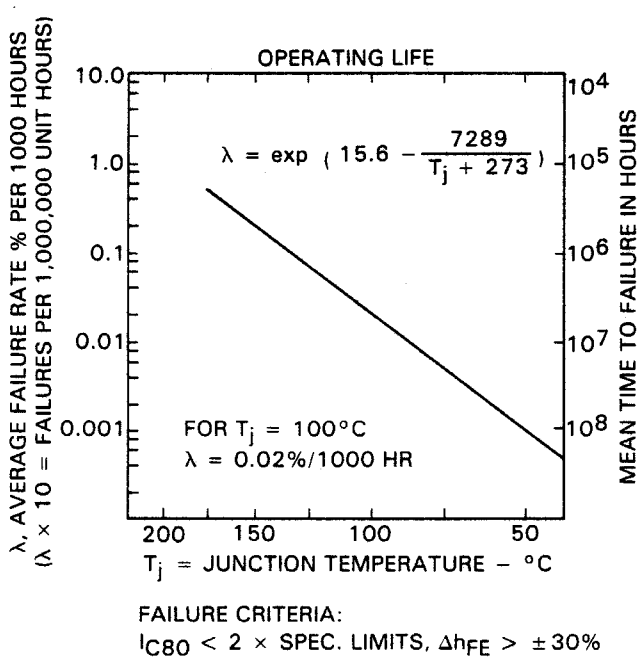
in this operating mode combine to yield a low failure rate and high reliability. Consequently, the reliability associated with this reverse-bias mode is not addressed in this paper.

In the bypass mode, a reduction in current-generating capability of cells within the group from shadowing, cracked cells, broken interconnects or other failures, causes the source current from other modules in the string to flow through the bypass diode. In this instance the voltage polarity across the group of solar cells is reversed and is limited to the forward voltage drop across the diode. The diode may perform its bypass function occasionally, if shadowing is caused by cloud cover or temporary maintenance obstructions, or continuously, if cracked cells or interconnect failures exist. In this mode, the diode may be required to conduct the worst-case source current, and the resulting diode junction temperature could exceed the maximum rated value if the diode is sized incorrectly or inadequately heat-sinked.

II. DESIGN CRITERIA FOR ACCEPTABLE FIELD RELIABILITY

The predominant failure mechanisms found in semiconductor devices are temperature-dependent and follow an Arrhenius model. Work by Herr et al has shown that higher junction temperature increases failure rates caused by degradation mechanisms such as ion migration, surface conduction, and metal corrosion.[4] Herr used an Arrhenius model (Figure 2) to determine the failure rate of plastic-encapsulated power transistors as a function of junction temperature. Note that a 50°C reduction in junction temperature reduces the failure rate by a factor of 10. Discussions of diode reliability by Shepard include the prediction of failure rates of silicon rectifying diodes typically used in PV bypass applications by stress-in-time tests, where



FAILURE CRITERIA:
$I_{C80} < 2 \times$ SPEC. LIMITS, $\Delta h_{FE} > \pm 30\%$

Figure 2. Failure rate of plastic encapsulated power transistors as a function of junction temperature using an Arrhenius model.

diode devices are evaluated at a constant stress as a function of exposure time.[1] Failure rate data from stress-in-time testing fit the Arrhenius model and relate failure-rate data to junction temperature. See data for a typical rectifying diode in Figure 3. Diode failure data from the MIL-HDBK-217D

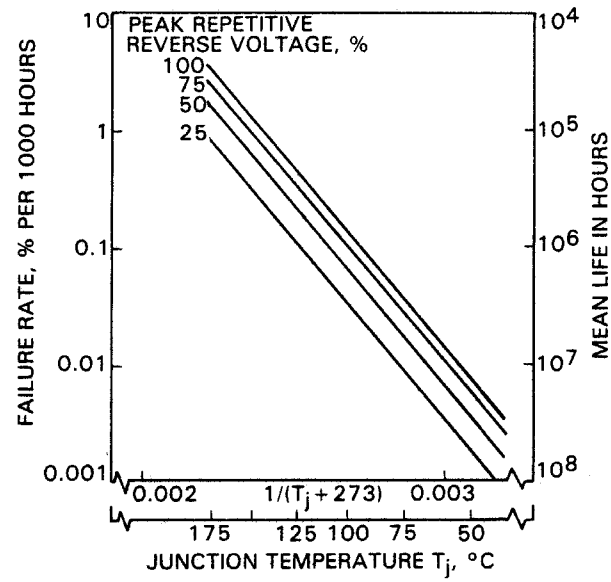


Figure 3. Failure rate for a typical rectifying diode.

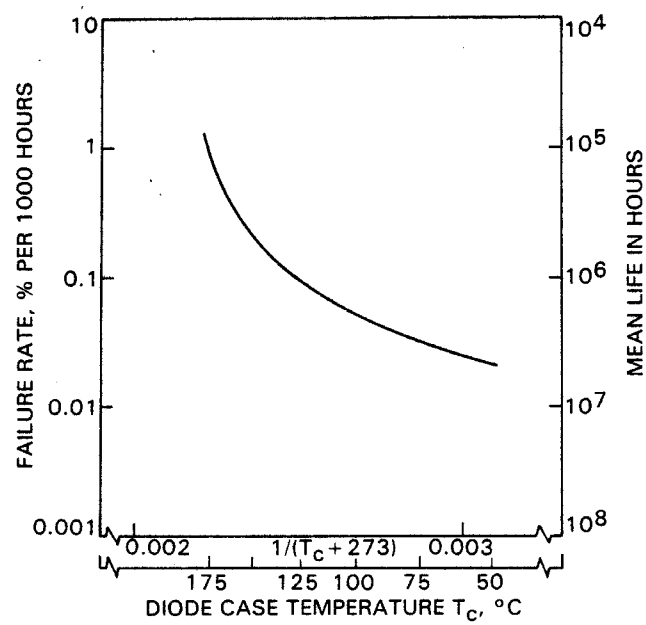


Figure 4. Failure rate of a silicon rectifying diode using MIL-HDBK-217D methodology.

method for predicting failure rates of discrete semiconductor devices are derived from the product of a base failure rate and various application-dependent modifiers (stresses).[5] The result does not follow an Arrhenius model, but failure rates are correlated with diode case temperatures (Figure 4). Further, semiconductor failure rates over time are also addressed by Herr with the usual "bathtub" failure pattern shown in Figure 5.[4] The workmanship failures occur during the burn-in

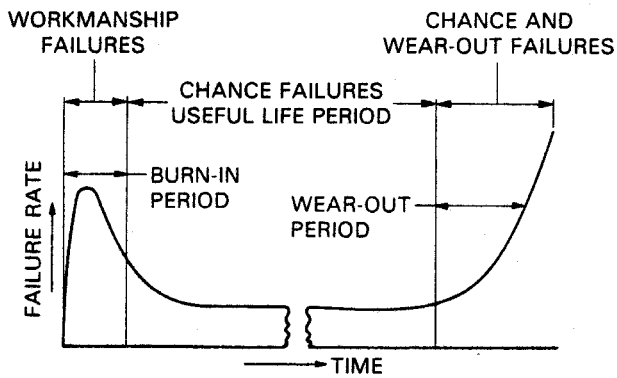


Figure 5. Semiconductor failure rate as a function of time.

period, and the wear-out-period failures are believed to be the result of basic design limitations. It is the chance failures during the longer useful-life period that are of most concern to PV designers. It follows that achieving long-term reliability requires that bypass diode junction temperatures be limited to the manufacturer's upper bound (maximum allowable value) under worst-case PV field thermal conditions and to a derated temperature, consistent with high reliability, during prolonged periods of high operating temperature. Based on SOLMET meteorological data and field observations across the U.S., field thermal conditions of 100 mW/cm^2 solar irradiance and 40°C ambient temperature can occur for extended periods. In addition, peak irradiance levels of up to 150 mW/cm^2 from cloud enhancement may be encountered during short periods. These peaks result in transient levels of high current up to 1.5 times the module short-circuit current (I_{sc}) at 100 mW/cm^2 and 40° C.

Based on the above mentioned considerations, it was decided to require that manufacturers' published maximum allowable junction temperatures not be exceeded under worst-case field conditions of 100 mW/cm^2 irradiance, 40°C ambient temperature, and a bypass current level of 1.5 times a module's short-circuit current at 100 mW/cm^2. To ensure long-term service, it is further required that junction temperatures be 50°C below the manufacturers' maximum allowables during prolonged periods of high operating temperatures. This is consistent with the standard industry practice of derating maximum temperatures to increase reliability. Specifically, the derated junction temperature is not to be exceeded under conditions of 100 mW/cm^2, 40°C ambient and 1.0 I_{sc}. The design criteria, summarized in Table 1, address a bypass diodes' maximum current and heat-sink adequacy, and are applicable to diode devices mounted integral with or external to the module.

III. METHOD FOR ASSESSING DESIGN CONFORMANCE

To assess conformance with the criteria in Table 1 it is necessary to have a test method for determining diode junction temperatures in situ under the specified thermal operating conditions. The following method was developed to meet this objective.

(1) Heat module front surface with infrared radiant heaters to obtain predicted module temperature rise above ambient for 100 mW/cm^2 irradiance conditions.

(2) Apply test current, 1.5 I_{sc} or 1.0 I_{sc}, to diode until thermal equilibrium is reached.

(3) Sense the diode junction temperature (T_j) by measuring forward voltage drop across junction at a fixed, known current level.

(4) Compute junction temperature under 40°C ambient conditions as T_j + 40°C minus the ambient temperature of test environment.

Each of these steps is discussed in detail in the following paragraphs.

Simulating Diode Thermal Boundary Conditions

To avoid having to generate a 40°C, 100 mW/cm^2 thermal test environment, the adopted procedure simulates the bypass diode's thermal boundary conditions by creating the proper temperature gradients between the diode, module and ambient test environment, and then adjusting the measured diode temperature for the difference between the ambient-test-environment temperature and the 40°C ambient temperature requirement.

Computing the required temperature rise above test-room ambient and correcting the measured

	Diode Junction Allowables	
	Maximum Temperature from Published Performance Data	Derated Temperature for Long-Term Reliability
Correlating Photovoltaic Field Conditions	100 mW/cm^2 Solar Irradiance 40°C Ambient Air Temperature 1.5 I_{sc} PV Module Short-Circuit Current at 100 mW/cm^2	100 mW/cm^2 Solar Irradiance 40°C Ambient Air Temperature 1.0 I_{sc} PV Module Short-Circuit Current at 100 mW/cm^2
p-n Diodes Schottky Diodes	175°C 125°C	125°C 75°C

Table 1. Design criteria for bypass diodes in photovoltaic applications.

junction temperature to a 40°C ambient is easily accomplished using standard photovoltaic Nominal Operating Cell Temperature (NOCT) relationships. Referring to Equation 1, a module's operating temperature (T_m) is the sum of the ambient air temperature and the thermal contribution from impinging solar irradiance. Industry standards exist for determining the module NOCT value, allowing convenient calculation of the contribution of irradiance.

$$T_m = T_a + KS \qquad (1)$$

where

T_m = module operating temperature, °C

T_a = ambient air temperature, °C

K = empirical constant characterizing the module's effective thermal resistance relative to its environment; K has a value of 0.36 for a typical photovoltaic module and is defined by the module's NOCT value at standard test conditions of 80 mW/cm^2, 20°C ambient; i.e., K = (NOCT - 20)/80

S = solar irradiance level, mW/cm^2

To obtain the predicted temperature rise above ambient during periods of 100 mW/cm^2 irradiance we use Equation 1 and the above definition of K; thus

$$\Delta T = T_m - T_a = \left[\frac{NOCT - 20}{80}\right] \bullet (100)$$

which gives

$$\Delta T = 1.25\ NOCT - 25^{o}C \qquad (2)$$

Equation 2 gives the module operating temperature rise above ambient for a solar irradiance level of 100 mW/cm^2. This predicted temperature rise above ambient can be duplicated in the laboratory using inexpensive infrared radiant heaters directed on the modules top (illuminated) surface.

By achieving module operating temperature first, the thermal interface between the module and the bypass diode installation is correctly simulated. For example, diodes embedded in the module laminate assembly are directly influenced by the module

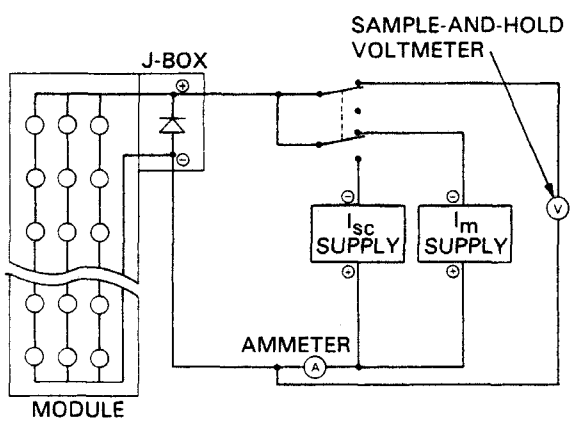


Figure 6. Test circuit for measuring bypass diode junction temperature.

operating temperature; externally mounted or integrally mounted diodes (in a junction-box) are indirectly influenced by T_m.

Because of the additive dependence of junction temperature on ambient air temperature, correcting for the difference between the test ambient and 40°C is accomplished by adding to the measured junction temperature as noted in step (4) of the procedure.

Application of Test Currents

After establishing the module thermal boundary conditions the test current is applied to the diode to raise its junction temperature to values consistent with the field source-current condition of 1.5 I_{sc} or 1.0 I_{sc}. Test currents may be applied using a test circuit as shown in Figure 6.

Junction Temperature Measurements

A diode's junction temperature can be sensed by obtaining the voltage drop across the junction from a fixed known current level that does not significantly heat the junction (further) during the sampling period. This necessitates a low level of measuring current (I_m) to be applied quickly to the junction immediately after removing the high test current (I_{sc}). The fast action switch (Figure 6) removes the high test current and directs the I_m current to the diode. The resulting voltage drop across the diode junction during application of I_m is then converted to a junction temperature by using the diode's voltage drop versus junction temperature characteristic curve. This diode characteristic is established from characterization tests by subjecting the external diode assembly or PV module to three or four oven temperatures and using the measuring current (I_m) to obtain voltage drop measurements at each temperature level.

IV. DEVELOPMENT OF PROCEDURAL STEPS

A series of exploratory tests were conducted on full-sizes modules, individual diodes, and assembly diodes (devices encapsulated as a package and attached to a heat sink) commonly used in PV applications to obtain procedural steps for the method. This test effort addressed a number of issues including diode voltage-temperature linearity and its dependence upon measuring and module currents (I_m and I_{sc}), test circuit and current switching intervals, laboratory thermal environment, and understanding the module operating temperature influence on junction temperatures of unencapsulated diodes.

Diode Characterization Tests

Axial, stud, and assembly diodes were used to obtain the forward voltage drop versus junction temperature characteristic for several measuring currents (I_m) ranging from 10 mA to 2 A. The I_m value and application interval selected for sensing junction temperatures could not increase the diode's junction temperature significantly. This required that the I_m value provide a good linear response with temperature and be significantly above a module's leakage current (without a bypass diode) in a dark environment. Oven tempera-

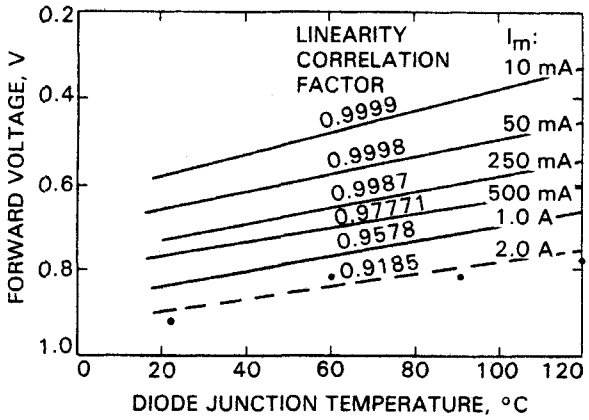


Figure 7. P-n diode junction temperature vs voltage drop characteristics for applied measuring currents (I_m).

tures of 120°C, 90°C, 70°C and a room temperature were used to obtain the linearity response and diode characteristics of forward voltage drop versus temperature for I_m values. In Figure 7, the diode characteristic curves for increasing levels of I_m were derived from a linear regression analysis; the resulting correlation factors (identifying linearity) are shown above. Note that precise (three-place to four-place accuracy) voltage drop measurements are required to obtain the high correlation factors. This necessitated a very stable power supply to deliver a constant measuring current (I_m) during voltage-drop measurements. Accurate voltage-drop measurements were easily obtained at I_m values up to 250 mA.

When applying measuring currents using the circuit shown in Figure 6, it is also necessary to identify the exact magnitude of I_m that passes through the diode, and that portion of I_m that leaks through the module's solar cells. Consequently, module leakage currents were characterized for a range of 0.5 V to 1.0 V reverse voltage as a comparison with the I_m values used in the diode characterization tests. Modules were laid face down on a flat table and then covered with a black velvet cloth. Figure 8 shows that leakage currents for the modules tested range from 81.7 μA to 0.57 mA and do not

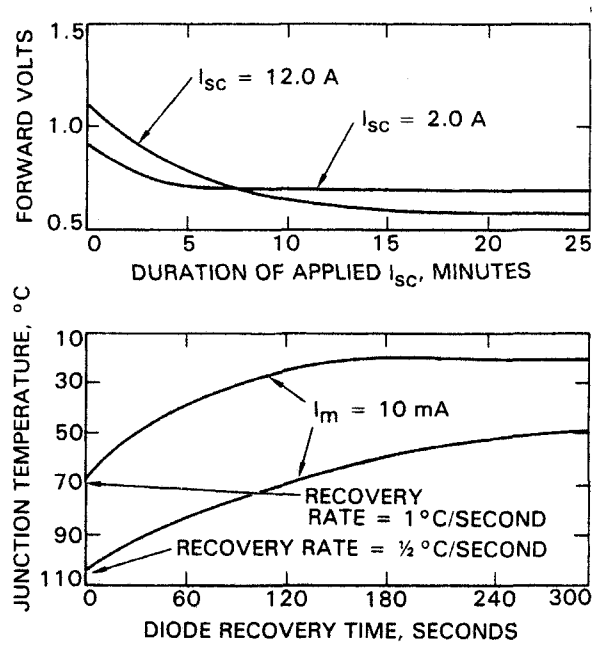
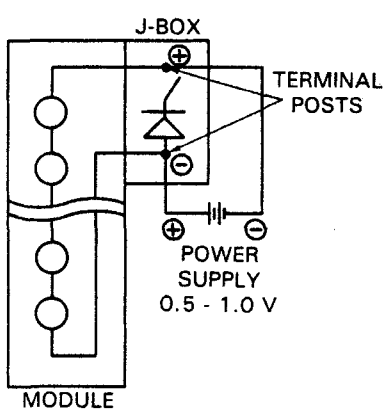


Figure 9. Diode response to applied I_{sc} and I_m currents.

increase significantly when the table surface is not perfectly flat. Therefore, I_m measuring currents kept in the 50 to 100 mA range are sufficiently above module leakage currents and are equally well suited for precise measurements during oven characterization tests.

A diode's thermal time-constant response to typical worst-case heating conditions is important for two reasons: first, for identifying required switching intervals from I_{sc} to I_m currents, and second, for determining the time necessary to achieve equilibrium conditions after application of the I_{sc} current. Diodes integral with the module typically bypass I_{sc} currents from 1.5 to 12.0 A and exploratory tests showed that a half-hour interval was sufficient to achieve equilibrium. However, tests with a 60 A external diode assembly required two hours to achieve steady voltage-drop readings. Diodes external to modules have to be addressed individually, considering the bypass



Results

Reverse Volts	Module Type 1 I (μA) Cover	1 W/O Cover	1 1/4 in. Tilt	Module Type 2 I (mA) Cover	2 W/O Cover	2 1/4 in. Tilt
0.5	81.7	81.7	82.2	0.57	0.57	0.59
0.6	—	—	—	0.68	0.68	0.72
0.7	113.4	113.4	113.7	0.79	0.79	0.83
0.8	129.3	129.3	129.6	0.91	0.91	0.94
0.9	144.5	144.5	145.6	1.02	1.02	1.05
1.0	160.6	160.6	163.5	1.13	1.13	1.18

Figure 8. Leakage current test results.

current level, heat-sink design, etc. Figure 9 shows the recovery rate from I_{sc} currents for two diode types indicating that a switching rate from I_{sc} to I_m currents should be on the order of 0.5 seconds.

Expanded Test Procedure

Using the above exploratory test results, an expanded test procedure was established based upon the test method:

(1) Determine diode forward voltage drop versus junction temperature characteristic curve at a chosen measurement current (I_m).

(a) Subject module or diode assembly (if external to module) to three oven temperatures: 60°C, 90°C, and 120°C.

(b) Select I_m value to provide good linear response with temperature (i.e., without heating the junction significantly) and at least two orders of magnitude above module leakage current (with PV cells in darkness).

(2) Measure voltage drop with module heating and I_{sc} current applied.

(a) Raise the module temperature to a value of (1.25 NOCT - 25°C) above room temperature with IR radiant heaters directed at the module front surface. The front of the module should be blackened to prevent illumination of the solar cells. Maintain normal installation distances between external diode assemblies and PV module.

(b) After the module and diode reach thermal equilibrium apply the test current (1.0 I_{sc} or 1.5 I_{sc}) to the diode while continuing the radiant heating flux established in (2a).

(c) After the diode again reaches thermal equilibrium (approximately 1/2 hour), instantaneously (< 1/2 sec) apply I_m and measure diode forward voltage drop. Repeat steps (b) and (c) for 1.5 I_{sc}.

(3) Determine diode junction temperature (T_j) under 1.0 I_{sc} and 1.5 I_{sc} currents by extrapolating 60°C, 90°C, and 120°C data (Step 1) .

(4) Translate each junction temperature (T_j) determined in Step (3) to correct for ambient temperature under worst-case field conditions (100 mW/cm^2, 40°C)and compare with Table 1 design criteria by using:

$$(T_j)_{100,\ 40} = T_j + 40^{\circ}C - T_{room}$$

PV Module Tests

To verify the method and expanded procedure, several PV modules were included in a series of prototype tests using the test circuit shown in Figure 6. Measuring currents (I_m) of 10 mA, 50 mA, and 100 mA were used with the above approach to obtain junction temperatures for heat-sinked diodes in several module configurations. Also, one diode assembly was in the test set; it is normally mounted externally to large PV panels and bypasses high (60 A) source currents.

Module Type	P-n Diode Location	NOCT[a] (°C)	T_{room} (°C)	1.0 I_{sc}[b] (A)	T_j at I_M = 10 mA (°C)	T_j at I_M = 50 mA (°C)	T_j at I_M = 100 mA (°C)
A	Across Terminals, In Junction-box	46	23.9	2.27	66.45	67.04	66.89
B	Bracket in Junction-box	54	23.3	12.02	106.65	104.65	105.40
C	P-C Board in Junction-box	49	26.4	5.30	151.47	150.28	151.73
D	Module Frame	56	24.4	6.80	119.36	118.90	121.90
E	Bracket in Junction-box	47	23.9	5.3	106.37	106.13	–
F	Across Terminals, in Potted Junction-box	51	23.9	1.44	41.95	40.73	39.37
G	External Assembly Diode	–	25.0	60.0[c]	96.54	–	–

[a] Module Nominal Operating Cell Temperature at Standard Conditions of 80 mW/cm^2, 20°C Ambient Air Temperature

[b] Module Short-Circuit Current at 100 mW/cm^2, 40°C Ambient Air Temperature

[c] I_{sc} of Panel Assembly

Table 2. Comparisons of junction temperatures (T_j) obtained from three measuring current (I_m) values for diodes under 1.0 I_{sc} module currents.

Individual temperature versus voltage drop diode characteristics were obtained for the module test set and diode assembly. The module diode voltage drop measurements were obtained after a one-hour soak at each oven temperature, which proved sufficient to reach equilibrium; however, this may vary with different oven facilities. Good linear responses were obtained at all levels of I_m from 10 mA to 100 mA for the diode characteristic curves.

A radiant heat source with a parabolic reflector was used to achieve the required module temperature in a local 4 ft^2 area that included the bypass diode. For the externally mounted diode assembly a large bank of radiant heaters was used to increase the module's temperature over a 12 ft^2 area. In this case the external diode and heat sink assembly were 18 in. from the module's back surface and received a limited amount of heating by radiation.

Thermocouples were used to monitor the module operating temperature and were installed on solar cells or back-cover materials. The time to reach thermal equilibrium varies with the heat source and laboratory conditions. However, thermal equilibrium for diodes integral with the PV module is achieved quickly ($\approx$1 hour) while external diodes may require longer periods (up to two or three hours) before the radiative and convective influences from the PV module stabilize.

Preliminary junction temperatures were obtained for the test set under 1.0 I_{sc} source current conditions with the same measuring currents (I_m) used in the characterization tests. Switching intervals from 1.0 I_{sc} to I_m were kept within 0.5 second to minimize measurement errors induced by device cooling rates. Measurement variations shown in Table 2 for 10, 50 and 100 mA levels of I_m are primarily within a 2% error.

Additional tests that remain in the development of the method include junction-temperature measurements on diodes under 1.5 I_{sc} source-current levels. Results from future tests are expected to identify which of the two allowable temperatures in the Table 1 design criteria is the more difficult to meet. The steps in the expanded approach will be further refined to establish a detailed qualification procedure based upon the method presented.

V. SUMMARY AND CONCLUSIONS

Specific design criteria for long-life service and high reliability of bypass diodes in PV applications have been identified for p-n and Schottky devices. A test method has been presented to assess conformance to the criteria and measure the relative reliability of bypass diodes. Additional testing is necessary to refine the procedural steps and to identify whether the diode maximum or derated allowable temperature is the more difficult design criterion.

From a photovoltaic designer's viewpoint, the method is convenient and provides easy assessments of junction temperatures using standard NOCT values and relationships. It also establishes the worst-case module-to-diode thermal interface, thereby accommodating different module designs and various diode mounting schemes, including those integral with and external to the module. Further, it is particularly well suited for determining diode junction temperatures in the field and can be useful in establishing a detailed low-cost qualification test procedure to assess installation adequacy of bypass diodes. The method will aid PV module and array designers in establishing adequate heat-sinks and making reliable diode selections.

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