

PHOTOVOLTAIC MODULE HOT SPOT DURABILITY
DESIGN AND TEST METHODS*

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ABSTRACT

The primary objective of the Jet Propulsion Laboratory's (JPL) Low-Cost Solar Array (LSA) Project is the development of low-cost flat-plate photovoltaic arrays. Part of the project includes a program to improve module and array reliability. This paper describes one aspect of this program, which investigates the susceptibility of flat-plate modules to hot-spot problems. Hot-spot problems arise in modules when cells become back-biased and operate in the negative-voltage quadrant, as a result of short-circuit current mismatch, cell cracking or shadowing. Significant degradation of array performance caused by local heating of cracked, shadowed or mismatched solar cells in field-deployed arrays has been experienced. A qualification test for determining the capability of modules of surviving these field hot-spot problems has been developed. Details of the test method, typical test results, and recommended circuit-design techniques for improving module and array reliability with respect to hot-spot problems are discussed.

INTRODUCTION

Field experience indicates that periodic circuit faults such as partial shadowing, cracking of cells, and interconnect open circuits must be expected to occur even in highly reliable arrays. Under these fault conditions it is desirable to ensure that possible hot-spot heating due to reverse biasing does not cause propagation of the fault or electrical safety hazards through such mechanisms as solder melting or encapsulant deterioration.

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Hot-spot heating is caused when module operating current levels exceed the reduced short-circuit current level of an individual cell or group of cells in an array circuit. The reduced short-circuit current fault condition can be the result of a variety of causes including nonuniform illumination (local shadowing), individual cell degradation due to cracking or soiling, or loss of a portion of a series-parallel circuit due to individual interconnect open circuits. Under this condition the cell(s) carrying the excess current dissipate power equal to the product of the current and the reversed voltage that develops across the cell(s), which can heat the cell(s) to elevated temperatures.

Analytical methods for estimating cell temperature due to back-bias conditions have been described in previous work (1,2). These methods provide a conservative approach for predicting the probability of occurrence of hot-spot problems. A logical extension of these analytical techniques has been the development of the qualification test and design recommendations described in this paper.

OBJECTIVES

The primary objective of this latter phase of the program was to develop suitable laboratory test procedures for evaluation of the hot-spot endurance of a module under a severe hot-spot field condition represented by the following assumptions:

- (1) Irradiance level = 100 mW/cm²
- (2) Ambient air temperature = 40°C
- (3) Module is at short circuit
- (4) Worst-case cell reverse I-V characteristics
- (5) Worst-case cell current mismatch resulting from fault conditions including cracks, shadowing or interconnect failure.

Secondary objectives of the program have been to investigate the relationship of $T_{cell} - T_{air}$ versus hot-spot power dissipation (mW/cm²) for several module configurations and cell sizes and to gather typical performance results for a variety of module constructions and cell sizes. The development of design recommendations and acquisition of engineering data useful to module designers in improving hot-spot endurance is the long range objective of this program.

HOT-SPOT TEST DEVELOPMENT

General Test Description

The hot-spot endurance qualification test evolved from a series of analytical and experimental studies of the problem. Development of the testing procedure entailed design and fabrication of a five-bay hot-spot test facility using dichroic filtered light sources (Type ELH), controlled constant-current-and-voltage power supplies, automatic timing and control circuitry and temperature and irradiance instrumentation. Figure 1 is a photo of one of the test bays.



Figure 1. Hot-Spot Test Facility

Rationale for Test Cell Selection. The degree of hot-spot heating within an affected cell is dependent on a variety of conditions, including the module series-parallelism, the amount of overall illumination, and the amount of over-current in the affected cell(s). Because the reverse-voltage I-V characteristics vary considerably from cell to cell within a given module, it is necessary first to determine the dark reverse voltage I-V curve for a representative sample of cells (at least 10) within the test module. This can be done by directly accessing individual cells or by obtaining data for multiple points using the shadow technique described by Hoffman and Miller (3). The cell's dark characteristics should be determined for reverse voltages from 0 to V_L or currents from 0 to I_L , whichever limit is reached first, where:

$$I_L = I_{SC} \text{ of an average cell at } 100 \text{ mW/cm}^2, \text{ NOCT.}$$

$$V_L = N \times V_{mp} \text{ of an average cell at } 100 \text{ mW/cm}^2, \text{ NOCT.}$$

N = Number of series cells per bypass diode or number of series cells per module, whichever is less.

V_{mp} = Voltage at maximum power.

When the family of reverse-voltage I-V curves is plotted for the representative sample of cells, a graph similar to that in Figure 2 should be obtained. The individual curves may be either all voltage limited (Type A), current-limited (Type B), or a combination of both (as shown). In general, the cells associated with the highest hot-spot heating levels are those with the highest shunt resistance, although low shunt resistance may be associated with extremely localized heating.

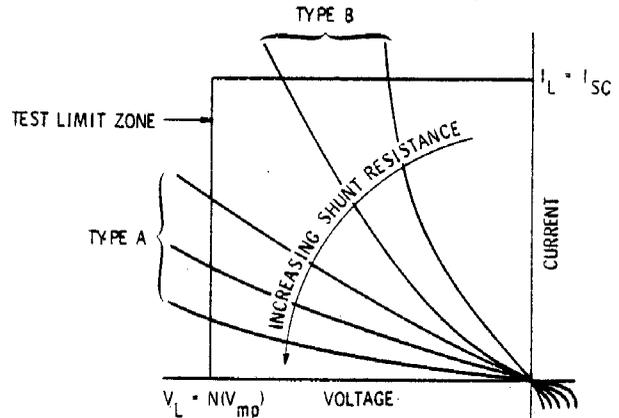


Figure 2. Test Cell Selection Based on Second-Quadrant Dark I-V Characteristics

For testing, three non-adjacent individual cells are selected within the test module from the measured sample: one representative of the highest shunt resistance obtained, one representative of the average, and one representative of the lowest. When the sample includes both A and B cells, the B type cell with the highest shunt resistance should be one of the selected test cells. The test cells are provided with positive and negative electrical leads to allow them to be connected individually to separate power supplies. Parallel current paths around the selected test cells are eliminated by disrupting cell-to-cell connections as necessary. Attachment of test leads is done so as to minimize disruption of the cell's heat-transfer characteristics or the integrity of the encapsulant system.

Selection of Hot-Spot Test Level

The purpose of this portion of the test procedure is to select the level of heating and the corresponding test condition that will stress the module in a manner similar to a severe hot-spot field condition. The severity of the field condition will depend on the array circuit configuration, the array I-V operating point, the ambient thermal conditions, the overall irradiance level, and the previously described characteristics of the affected cells. In particular, whether the cells are Type A or Type B is important.

For Type A Cells. The maximum cell reverse voltage (V_L), the cell illumination level, and the ambient thermal environment are the key parameters. When a module is incorporated into an

array branch circuit, the maximum reverse voltage imposed on an individual cell can approach the maximum array operating voltage if bypass diodes are not used. In this procedure it is assumed that the array designer has used bypass diodes or other means to limit the reverse voltage on any single module to less than one volt. The test voltage (V_{test}) is thus set to yield the maximum reverse voltage that would be applied across a single cell if the test module were operated at or near short circuit. Small cracks or shadows on this type of cell lead to the highest levels of deposited power (Figure 3). For Type A cells, V_{test} is therefore set equal to N times the average V_{mp} of an individual cell, where N is the number of series cells per bypass diode, or the number of series cells per module, whichever is less.

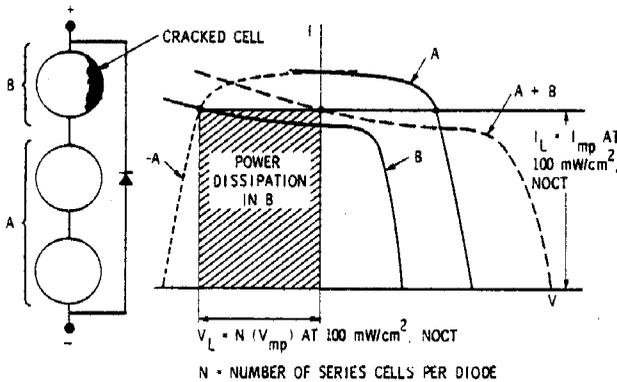


Figure 3. Selection of Test Voltage and Current for Type A Cells

The second key test condition for Type A cells is the illumination level; it directly controls the hot-spot test current (I_{test}) level, and therefore the power level. As shown in Figure 4, there is a unique illumination level that corresponds to worst-case power dissipation for any particular Type A solar cell. This occurs when the cell reverse bias voltage is equal to V_L at the test current (I_{test}). The irradiance level on the test cell shall be adjusted to achieve this worst-case condition with I_{test} set equal to the average cell maximum power current at 100 mW/cm^2 , NOCT.

The third test condition is the level of the ambient thermal environment. For test purposes a nominal terrestrial environment is created by using an air temperature of $20^\circ \pm 5^\circ\text{C}$ and a radiant heating source to achieve a uniform background module cell temperature equal to NOCT. The combination of raising the test cell temperature to NOCT (equivalent of 80 mW/cm^2) plus establishing the deposited power levels yields a simulation of the desired 40°C field ambient condition.

Type B Cells. Type B cells have a cell shunt resistance so low that the maximum reverse test voltage (V_{test}) is set by the I-R drop across the cell associated with the available current level. In these cells, worst-case heating occurs when the test cell is totally shadowed, and the current level is at a maximum. This situation is

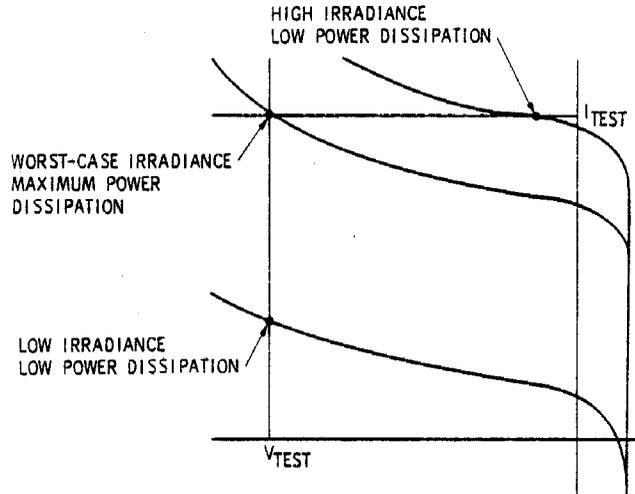


Figure 4. Selection of Illumination Level to Control Degree of Reverse Biasing in Type A Cells

illustrated in Figure 5 in which it is seen that the reverse voltage will increase at maximum current as shadowing increases. Test conditions for Type B cells therefore maintain a cell illumination level of less than 5 mW/cm^2 (to allow for room lighting and an IR heating source) "and I_{test} equal" to the short-circuit current of an average cell at 100 mW/cm^2 , NOCT. As with Type A cells, a uniform background cell temperature equal to NOCT shall be created by using an air temperature of $20^\circ \pm 5^\circ\text{C}$, together with a radiant heating source.

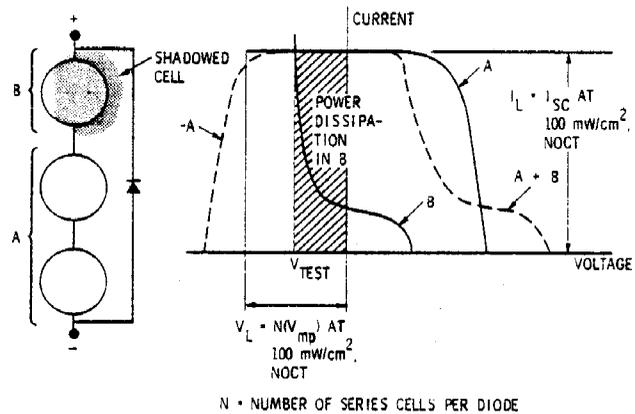


Figure 5. Selection of Test Voltage and Current for Type B Cells

Selection of Test Sequence and Duration

The selected test cells are subjected to a cyclic (on-off) sequence for an accumulated power-on duration of 100 h. The cyclic heating (1 h on followed by sufficient off-time to allow the test cells to cool to within 10°C of NOCT) is intended to simulate the daily occurrence of hot-spot heating conditions within the module. The 100-h

duration is based on the results of the exploratory tests, which showed that for some module designs known to have hot-spot heating problems in the field, at least 60 h of on-time testing was required before similar problems were observed on the laboratory test articles. The 100-h duration provides reasonable assurance that hot-spot heating effects, including delamination, outgassing or blistering of encapsulants, cell cracking, or solder melting can be observed.

Test Execution

Detailed steps for execution of the test involves subjecting the three selected test cells to cyclic hot-spot heating, at the levels determined above, for a period of 100 h total on-time, as follows:

- (1) Connect a separate dual limiting constant-current/constant-voltage power supply to each test cell with polarity arranged to drive the cells with reverse voltage. Adjust the voltage and current limits to the V_{test} and I_{test} values determined above.
- (2) Apply an IR radiant-heating source with a visible light contribution below 5 mW/cm^2 to the module front surface and adjust the heating level to achieve a uniform module cell temperature equal to NOCT $+2^\circ\text{C}$. The ambient air should be still and at a temperature of $20^\circ \pm 5^\circ\text{C}$.
- (3) For Type A cells only, arrange an additional light source to illuminate each test cell to the unique level determined above and illustrated in Figure 4. This is most easily accomplished after the power supply and IR source are initially turned on by adjusting the illumination level to achieve, simultaneously, both current and voltage limiting at I_{test} and V_{test} after equilibrium test conditions stabilize. The illumination source should not contain excessive infrared or ultraviolet irradiance that would lead to abnormal heating or accelerated UV aging. ELH-type tungsten sources have been found to meet this requirement.
- (4) Connect the power supply, IR source, and light source to an appropriate timer to obtain a cyclic on-off operation with an on-time equal to 1 h, and an off-time sufficient to allow the test cells to cool to within 10°C of NOCT.
- (5) Conduct the test until a total of 100 h of on-time has been accumulated.
- (6) Inspect the test cells and adjacent areas of the encapsulation system visually at 24-h intervals during the test while under bias conditions, and upon completion of the 100 h sequence. Identify any evidence of degradation, including delamination, outgassing or blistering of encapsulants, cell cracking, solder melting or other defects. Usually a post-test electrical performance test is

conducted (after re-connecting any disrupted parallel connections) for comparison to module and cell initial performance.

LABORATORY TEST RESULTS

The laboratory tests performed in support of the hot-spot test development have provided results that give insight into the response of modules to hot-spot power dissipation. The ability to predict and understand module response is important for several reasons. First, the module circuit configuration determines the level of hot-spot power dissipation. Secondly, the material composition determines the endurance to the subsequent temperature increase. Therefore, module and array designers would benefit from guidelines relating their module characteristics to the potential for hot-spot problems.

An important aspect of the hot-spot endurance test is the time required for the module to reach equilibrium temperature after being brought to a reverse-bias condition and, again after the reverse-bias voltage is removed. These time constants are significant in determining the time of the reverse-bias cycle and the time required for cool-down afterwards. A set of typical curves (Figure 6) were determined in the laboratory for three representative mini-modules and show that the time required to reach equilibrium is on the order of 10 to 20 minutes.

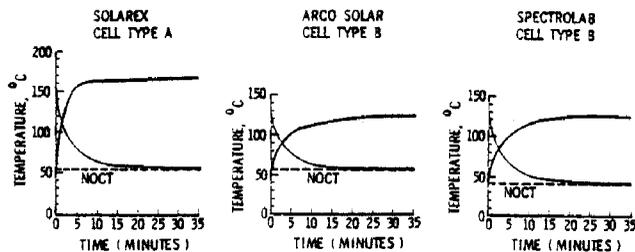


Figure 6. Time to Reach Equilibrium Temperature

The laboratory tests involved the use of a camera sensitive to infrared (IR) radiation to determine the cell hot-spot temperature distribution in conjunction with the use of a type E thermocouple. The thermocouple was affixed to the back of the cell and the IR camera was used to measure front-surface temperature. Because of front-to-back thermal gradients through the module and uncertainties in front-surface emissivities, exact agreement between the IR camera and the thermocouple readings would not be expected to agree precisely. In addition, the affected cell has a temperature gradient (non-concentric with the cell center) above its surface and, therefore, the thermocouple reading and the highest hot-spot temperature on the cell would not ordinarily be expected to coincide. However, correlations of thermocouple and infrared measurements have provided comparative data.

Two sets of measurements were made with a typical set of representative modules. These

measurements were made at an ambient temperature of $20^{\circ}\text{C} \pm 5^{\circ}\text{C}$. The first set was made by causing a given level of electrical power to be dissipated in the affected cell with the module initially at room temperature. The second set of measurements was made with the module initially at the NOCT temperature. The second set was meant to simulate the actual hot-spot endurance test described earlier in this paper.

In each set of the measurements the procedure was identical except for initial temperature, as noted above. The IR camera is focused on the desired area of the module. One of the modes of use of the IR camera is in conjunction with a video display, where a sharp black-and-white contrasty video image of the subject is displayed; in this case an area at a given uniform temperature is displayed as one shade and all other areas (any other temperature) are displayed as the opposite shade. Multiple exposures can be taken with a Polaroid camera as the temperature under display is varied. In this way an image of alternating white and black areas is obtained, each at a given temperature, thus providing a pseudo-isothermal representation of cell gradients and permitting determination of the maximum hot-spot temperature. This technique was used to obtain a range of temperature gradients across a hot-spot cell and the module containing it. This information was then used in conjunction with the thermocouple on the cell to estimate the hot-spot (highest) cell temperature. The highest cell temperature was estimated by considering the relationship of thermocouple- and IR camera-derived temperatures and the locations of the appropriate areas when projected on the surface of the cell.

A variety of module construction configurations, were employed in verifying the hot-spot test procedure and gathering design data, as shown in Figure 7. Figure 8 was plotted from data taken using five typical modules, starting at room temperature. The difference between the cell hot-spot temperature and the ambient air temperature is plotted along the ordinate. This gives a measure of the highest temperature experienced by any point on the cell relative to the ambient temperature. This set of plots is meant to be used to estimate the expected cell temperature increase over ambient in a field environment. Stultz and Wen have shown that the change in $T_{\text{cell}} - T_{\text{air}}$ is linear with respect to irradiance and hence selection of a worst-case ambient temperature of 40°C permits direct calculation of the maximum expected cell temperature (4).

The temperature difference is plotted against the total power per unit area being dissipated into the cell on the lower axis, and ratio of the total power deposited in the cell to the maximum power output of a normal cell. The total power dissipated includes the electrical power supplied by the power supply, and the power supplied by the lamp illuminating the cell, if any. Also plotted in the figure is a curve used in the workbook supplied at a photovoltaic circuit design workshop held at JPL in April and May 1980 (2). This

MODULE MFG	MODULE CHARACTERISTICS
SOLAREX	GLASS-FIBER-REINFORCED POLYESTER SUBSTRATE SYLGARD 184 ENCAPSULANT ALUMINUM FRAME CELL SIZE: 3 in.
PHOTOWATT	ALUMINUM SUBSTRATE GLASS SUPERSTRATE RTV 615 ENCAPSULANT ALUMINUM FINIS CELL SIZE: 2.2 in.
ARCO SOLAR	GLASS SUPERSTRATE PVB ENCAPSULANT ALUMINUM FRAME CELL SIZE: 3 in.
SOLAR POWER	GLASS REINFORCED POLYESTER SUBSTRATE SYLGARD 184 ENCAPSULANT CELL SIZE: 4 in.
SPECTROLAB	GLASS SUPERSTRATE PVB ENCAPSULANT ALUMINUM FRAME CELL SIZE: 2 in.

Figure 7. Characteristics of Modules Tested

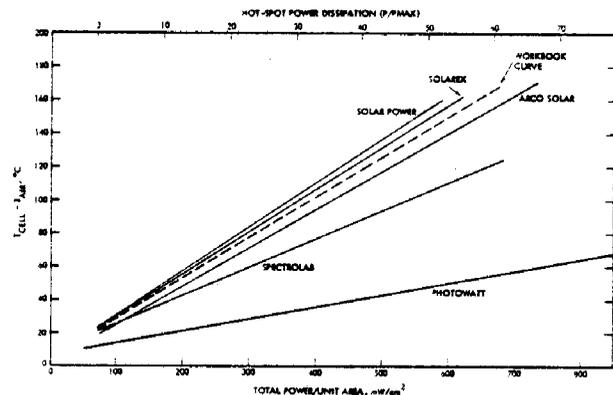


Figure 8. Predicted Hot-Spot Field Temperature Above Ambient vs Power Into a Cell

curve, which was derived from early cell hot-spot temperature measurements at JPL, has been used extensively to predict the level of hot-spot heating in modules of a given circuit configuration used in arrays of a given circuit configuration. Except for one module, the modules tested ranged about the workbook curve (Figure 8). The module curves shown were drawn through a scatter of points resulting from tests made with different cells in each module. However, the use of the workbook curve will generally lead to nominal estimates of hot-spot temperatures. When specific design data for a module of interest is available, it should, of course, be used in this analysis.

As discussed above, the amount of power dissipated in a back-biased cell is a function of the second-quadrant cell I-V characteristics and the series-parallel configuration of the module. The actual temperature rise in the cell and surrounding area of the module is a function of the thermal characteristics of the materials of which the module is constructed. With regard to second-quadrant characteristics, the plots in Figure 8 represent the average of several cells in each module. Therefore, each curve represents a straight-line fit to a scatter of data points for a particular module. A comparison of the expected temperature rise for several different module construction configurations can be made.

Figure 9 provides the results of a second set of measurements, which were meant to simulate the hot-spot endurance test. In this case each curve represents the results from a single cell. For those modules for which both Type A and Type B cells were available for testing, the results for one of each type are presented in the figure. In each case the cell and surrounding module area were first brought to equilibrium at NOCT. Next the test cell was subjected to power dissipation, consisting of an electrical input and in the case of a Type A cell an illumination power input.

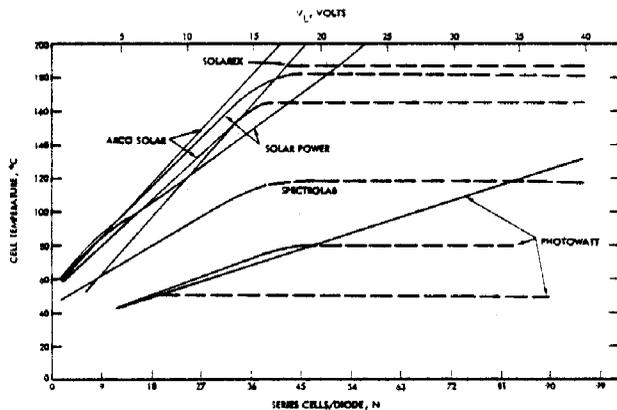


Figure 9. Measured Hot-Spot Temperature vs Number of Series Cells per Diode

The actual cell equilibrium temperature reached is plotted as a function of the number of cells in series with the cell in question (assuming a bypass diode around the cells). The number of series cells per diode is used to determine the voltage drop across the affected cell. Because only the voltage across a back-biased cell, and not the current through the cell, is a function of the number of cells in series, the power dissipation increases with the number of cells in series (i.e. directly with the increase in voltage). For Type A cells the voltage increase will continue as the number of cells increases (within the number of cells in a module). For Type B cells, the voltage cannot increase beyond that value of voltage for the maximum current possible passing through the cell. Therefore, the maximum power dissipation will reach a limit as the number of series cells

is increased beyond that number corresponding to the voltage at the maximum cell current. Thus, those curves corresponding to Type B cells in Figure 9 level off at some point. Also, for reference purposes, the voltage across the back-bias cell corresponding to the number of series cells along the lower axis for an assumed V_{mp} of 0.42 volts is plotted along the upper horizontal axis.

The 200°C upper limit on the plots of Figures 8 and 9 is selected because the melting point of solder is in the range 180 to 200°C and module reliability would be greatly reduced beyond this temperature. Since the curves are based on individual cells, there is some overlap of the curves. However, there is enough of a trend in these estimates to allow separation of the hot-spot endurance capability according to module type.

The actual module response (visual only) as a function of temperature is given in Figure 10 for the five module types tested. Several types of effects were noted. One of the most common and most serious consequences of hot spot heating is cell cracking. The second commonly noted effect is encapsulant deterioration including outgassing and bubble formation (carbonation), discoloration, melting and delamination. Another effect of back-biasing is cell shorting. This is actually a safety relief valve when it occurs, since the power dissipation becomes negligible and cell temperature decreases. The cell, however, typically remains shorted after power is removed. Some modules survived to high temperatures without visible effects.

MODULE MFR	CELL HOT-SPOT TEMPERATURE °C				
	100	120	140	160	180
SOLAREX			CELL BREAKDOWN		CRACKED CELL
PHOTOWATT					CELL BREAKDOWN
ARCO SOLAR	ONSET OF CARBONATION		CARBONATION OVER HALF OF CELL		ENCAPSULANT DISCOLORED AND SMOKING
SOLAR POWER			MULTIPLE CELL CRACKS AND ENCAPSULANT DELAMINATION		ONE CELL SURVIVED TO 180 °C BEFORE CRACKING AND SHORTING
SPECTROLAB		ONSET OF CARBONATION			CARBONATION OVER ENTIRE CELL AREA

Figure 10. Observed Module Response vs Cell Temperature

MODULE DESIGN RECOMMENDATIONS

The work described in the last section forms a basis for developing preliminary module design recommendations for hot-spot endurance. In particular, the engineering data provided in Figures 8, 9, and 10 can be applied immediately to a variety of module designs. The hot-spot susceptibility of a module can be reduced by limiting the number of series cells per diode and/or by module construc-

tion. Figure 9 offers a basis for this type of design trade-off. The number of cells per bypass diode, as a general rule, should be no more than 12 to 15. Results of the tests performed indicate that this will limit hot-spot temperatures to values less than 120°C for a 40°C ambient temperature and 100 mW/cm² insolation level. An example of the use of these data to calculate the expected maximum cell temperature is presented in Figure 11. This example also indicates the agreement of the laboratory test method with predicted field results.

- KEY MODULE AND CELL PARAMETERS
 - 4 in. CELLS, 103.2 cm² OF AREA
 - 36 CELLS, 1 DIODE PER MODULE
 - V_{MAXP} (NOCT) = 0.42 V
 - I_{SC} = 2 A
 - TYPE A CELL
- V_L = 15 V, I_L = 2 A
- AT 0 ILLUMINATION, CURRENT AT 15 V IS 0.25 A

<p>CELL TEMPERATURE - LABORATORY ENVIRONMENT 20 °C AIR TEMPERATURE</p> $P_e = \frac{\text{POWER}}{\text{UNIT AREA}} = 30\text{W}/103.2 \text{ cm}^2 = 291 \text{ mW/cm}^2$ $P_{ILL} = \frac{(I_{LL} = I_L - 0.25\text{A})}{I_L} \times 100 \text{ mW/cm}^2 = 87.5 \text{ mW/cm}^2$ <p>NOCT EQUIVALENT = 80 mW/cm²</p> $P_T = P_e + P_{ILL} + 80 \text{ mW/cm}^2 = 458.5 \text{ mW/cm}^2$ <p>T_{CELL} - T_{AIR} = 120 °C, T_{CELL} = 140 °C</p>

<p>CELL TEMPERATURE - FIELD ENVIRONMENT 40 °C AIR TEMPERATURE</p> $P_T = P_e + 100 \text{ mW/cm}^2 = 391 \text{ mW/cm}^2$ <p>T_{CELL} - T_{AIR} = 100 °C, T_{CELL} = 140 °C</p>

Figure 11. Example Calculation of Expected Hot-Spot Temperature

FUTURE WORK

As a follow-on effort, an extensive thermal analysis involving the tests and an analytical model is under way. The thermal test involves an in-depth thermal mapping of a module in which a cell is subjected to hot-spot heating. Both thermocouples and IR data are being used. The data obtained are being used in an analytical model in order to identify the module parameters to which its thermal response are most sensitive. These parameters could include such things as encapsulant thickness and conductivity, glass thickness, module back insulating material characteristics, and surface emissivities.

REFERENCES

1. Gonzales, C., and Weaver, R., "Circuit Design Considerations for Photovoltaic Modules and Systems," Proceedings of Fourteenth IEEE Photovoltaic Specialists Conference, San Diego, California, January 7-10, 1980.
2. Proceedings of the Flat-Plate Photovoltaic Module and Array Circuit Design Optimization Workshop, JPL Internal Document 5101-170, Jet Propulsion Laboratory Pasadena, California, May 19 and 20, 1980.
3. Hoffman, A.R., and Miller, E.L., Bias-Humidity Testing of Solar Cell Modules, JPL Internal Document 5101-84, Jet Propulsion Laboratory, Pasadena, California, October 15, 1978.
4. Stultz, J.W., and Wen, L.C., Thermal Performance Testing and Analysis of Photovoltaic Modules in Natural Sunlight, JPL Internal Document 5101-31, Jet Propulsion Laboratory, Pasadena, California, July 29, 1977.