

PHOTOVOLTAIC MODULE AND ARRAY RELIABILITY

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ABSTRACT

Several statistical reliability studies have been conducted in areas of photovoltaic component design covering cell failure, interconnect fatigue, glass breakage and electrical insulation breakdown. This paper integrates the results from these various studies and draws general conclusions relative to optimal reliability features for future modules. The described analysis is based on designing for specified low levels of component failures and then controlling the degrading effects of the failures through the use of fault tolerant circuitry and module replacement. Means of selecting the cost-optimal level of component failures, circuit redundancy, and module replacement are described.

INTRODUCTION

The reliability of photovoltaic solar arrays is probably second in importance only to cost in the list of factors influencing the market acceptance of this new technology. Because of their uniquely modular nature photovoltaic arrays possess a higher than normal sensitivity to common-mode failures, but at the same time offer a wealth of redundancy options to increase reliability. Achieving the high reliability demanded by large-scale application will require that these unique reliability design attributes be well understood and utilized effectively.

As part of the Jet Propulsion Laboratory's Low-Cost Solar Array project a comprehensive array engineering activity has been directed to understanding the reliability attributes of terrestrial flat-plate photovoltaic arrays and to deriving analysis and design tools useful for array optimi-

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zation and cost reduction. This paper provides an overview of the array reliability problem, and defines a rational approach to achieving high reliability at minimum cost.

At the root of the reliability problem is the need to electrically interconnect literally thousands of nearly identical solar cells in series and in parallel to achieve the voltage and current levels of the intended application. For example, a typical 250-volt residential array will require 500 to 600 series cells, and a typical 1500-volt central station application will require 2000 to 3000. This large number of series elements makes an array extremely sensitive to infrequent cell failures unless a high level of circuit redundancy is utilized.

The reliability engineering problem is thus to achieve a high level of reliability at low cost by optimally trading off the available solution strategies. These include defining and achieving the appropriate piece part failure rates for the cells and interconnecting components, designing the appropriate levels of fault tolerance into the array circuit, and selecting the optimal maintenance/replacement strategy. In the remainder of this paper each of these solution strategies is explored and then combined to define least-cost solutions based on minimum life-cycle energy cost for the total system.

CONTROLLING PIECE PART FAILURES

A first solution strategy centers on controlling component failure mechanisms and rates. These are most easily considered in two categories: those generally associated with failure at the solar cell level, and those associated with failure at the module level. Solar cell failures are primarily cell cracking, interconnect open circuits and increased cell metallization contact resistance.

Cell Cracking

Of the cell failures currently seen in the field cell cracking is by far the most prevalent and is occurring at a rate of about 1% per year (Table 1). Although only 0.1 to 0.01 of these cracked cells have resulted in open-circuit cell failures, even this small (0.0001) failure rate can

Table 1. Cracked and failed cells due to field exposure.

SITE	TOTAL NUMBER OF CELLS IN FIELD	FRACTION* CRACKED PER YEAR	FRACTION FAILED PER YEAR
MEAD NEBRASKA	90,168	0.010	0.00021
MT. LAGUNA CALIF.	96,236	0.025	0.0010

lead to substantial array power degradation. Reducing the power degradation by further reducing the cell failure rate is a difficult task because of the unavailability of predictive design techniques to determine when a design has achieved a desired failure level. Present rates have been quantified only after expensive auditing of actual field performance.

The three primary causes of cell cracking appear to be differential expansion between the cell and its support, impact loading by hailstones, and reduced strength due to cell damage occurring during cell processing and module assembly. Although qualitative design techniques exist which address the first two causes (1,2), cell strength data are only available for near average cells (Figure 1) (3). This lack of strength and stress data on the one worst case cell out of a thousand places a high reliance on test techniques such as those defined in Reference 4 and on the use of fault tolerant circuitry such as multiple cell interconnects.

Cell Interconnects

Cell interconnects are both an important tool for reliability improvement and a source of failures. Given that a cell has cracked or otherwise degraded in a local area, the extent of module or array degradation can be substantially lessened by electrically attaching to the cell at more than one location. One means of assessing the degree of improvement possible is to consider analytically a large number of randomly oriented potential cracks and then to determine the fraction which would lead to open-circuiting or significant (10%) cell degradation (area loss). Table 2 illustrates the results of applying this Monte Carlo technique to a variety of interconnect geometries and indicates that substantial improvements can be achieved. Many of the latest module designs are taking advantage of multiple interconnect attachment points and are expected to have substantially reduced failure rates. With present cell failure rates at about 0.0001 per year (Table 1) it is expected that the improved redundancy will lead to values approaching 0.00001 per year.

The above optimistic projection of course assumes that the interconnects themselves don't

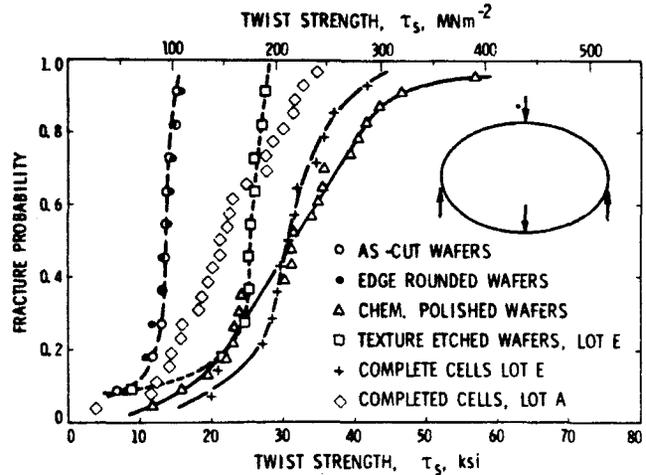


Figure 1. Effect of cell processes on the twist strength of silicon wafers and cells

fail, and of course they do. Interconnect open circuiting due to mechanical fatigue is a historical photovoltaic array failure mode and has even recently taken its toll on some modern installations. Like cell breakage, it is primarily caused by thermal and humidity expansion differences between the cell and its supporting substrate or superstrate. Also like cell breakage, interconnect fatigue is not easily predicted by available analytical models until the level of failure reaches major proportions. Mon and Moore (5), for example, have shown that the work of Manson (6) together with finite element stress analysis of the cell interconnect provides excellent prediction of the number of cycles required to result in the failure of 50% of the interconnects. In work with this author, they have empirically characterized the probability of failure of a variety of photovoltaic interconnects versus number-of-cycles (Figure 2) and developed a fatigue curve which treats probability-of-failure as a parameter (Figure 3). As can be seen from Figure 2, even carefully shaped interconnects can be expected to fail over a broad range of cycles, the weakest failing one hundred times sooner than the average.

Table 2. Fraction of cracked cells leading to failed cells for various multiple cell contacts

PERCENT LOSS OF CELL AREA	0°	60°	90°	-180°	+	-
0-5	.36	.42	.50	.64	.36	.91
5-10	.09	.15	.18	.18	.14	.09
10-20	.06	.12	.12	.12	.12	0
20-40	.03	.06	.06	.06	.11	0
40-70	0	0	0	0	.04	0
100	.45	.24	.14	0	.23	0
SUM OF ≥ 10	.54	.42	.32	.18	.50	0

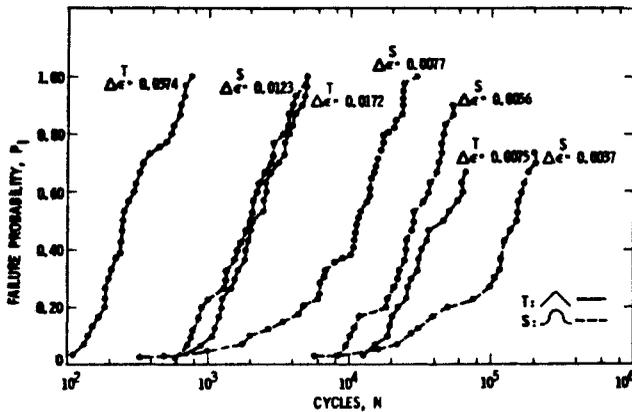


Figure 2. Cyclic mechanical fatigue test data for two copper interconnect shapes (T,S) and peak-to-peak strains ($\Delta\epsilon$)

As with cell cracking, the solution is to design for a manageable number of failures (maybe 10% during the array's design life) and then to incorporate interconnect redundancy to control power losses associated with those that fail. For example, if 3 interconnects were used to connect each cell, failure of 10% of the interconnects would lead to a cell failure density of one per thousand at the array design life.

Module-Level Failures

In addition to failure modes which are best treated at the cell level there are a number of failures which are more appropriately considered at the module level. These include glass breakage, electrical insulation breakdown and various types of major encapsulant failure such as delamination. Like cell failures, these failures are also probabilistic in nature and must be treated as such when considering quantities of modules in a large array. Moore (7) and Mon (8) in work with the author have developed empirical/analytical tools for designing for given statistical levels of glass breakage and electrical breakdown, respectively. Both of these failure mechanisms are flaw-related and therefore statistical in nature. When designing for appropriate levels of module failures it is important to note that a module failure is likely to cause an electrical hazard or major power loss and will therefore require immediate maintenance or replacement. As a result, module failure rates are traded off against life-cycle maintenance costs as opposed to redundancy and life-cycle energy loss, which are associated with cell failures.

FAULT TOLERANT CIRCUIT DESIGN

Given that the component failure rates have been reduced to manageable levels, it is necessary to introduce various circuit redundancy features to control the effect of the remaining few failures on module yield and array power degradation.

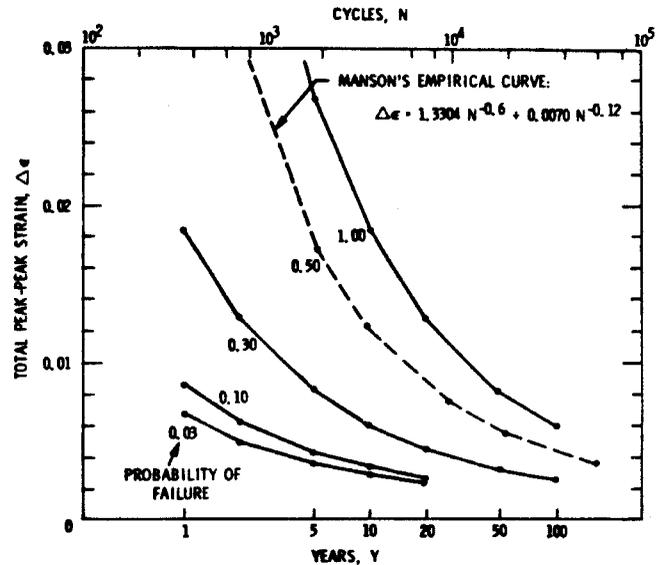


Figure 3. Interconnect strain-cycle fatigue curves with failure probability as a parameter

Array Degradation

The first step toward circuit redundancy is generally associated with dividing the large matrix of cells which makes up the array into a number of parallel solar cell networks referred to as "branch circuits." The branch circuits provide convenient points for monitoring array performance and provide an ability to isolate small areas of the total array for maintenance and repair. As shown in Figure 4, each branch circuit may contain a single string of series solar cells or a number of parallel strings interconnected periodically by cross ties. The cross ties divide each branch circuit into a number of "series blocks." One or more series blocks may also be bridged by a "bypass diode" which is designed to carry the branch-circuit current in the event that local failures constrict the current flow to the point of voltage reversal and power dissipation.

It is the use of series/paralleling and bypass diodes in the individual branch circuits which is key to controlling array degradation. Four parameters are of particular importance—the number of parallel strings, the number of series blocks per branch circuit, the number of series blocks per bypass diode, and the number of cells per substring within each series block.

A key problem in making use of these circuit redundancy features has been in quantifying the influence of specific series/parallel and bypass diode arrangements on array degradation. This problem has been solved recently by the development of an elaborate parametric analysis based on the statistical distribution of failed substrings due to random cell open-circuit failures (9, 10). Given a specific branch circuit configuration, the substring failure

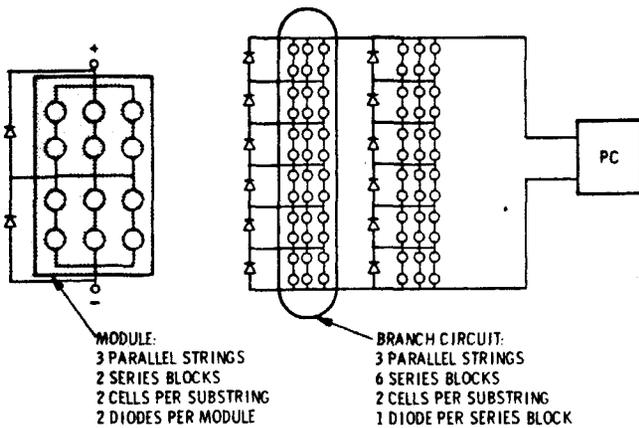


Figure 4. Series-parallel nomenclature

density (F_{SS}) can be computed easily from the cell failure density (F_C) and the number of cells per substring (n) using the following statistical equation:

$$F_{SS} = 1 - (1 - F_C)^n \quad (1)$$

Reference 10 contains a large number of parametric plots, an example of which is shown in Figure 5, which allow rapid computation of the effects of circuit redundancy on array power loss.

To obtain an assessment of the level of reliability improvement which can be achieved, it is instructive to consider the problem of calculating the expected power degradation after five years for a 1000-volt large ground-mounted array with one cell failure per 10,000 per year. To achieve the 1000-volt nominal operating voltage requires approximately 2400 series solar cells per branch circuit. Let us assume further that the array is composed of 1.2 m x 1.2 m (4 ft x 4 ft) modules each containing 144 solar cells. If the modules contain a single series string of 144 cells and no bypass diodes, each branch circuit could be made up of 17 series modules giving a total of 2448 series cells.

Calculation of the expected array degradation after 5 years can be accomplished using Figure 5 by noting that the assumed configuration is identical to eight parallel cells by one series block. However, Equation 1 must first be utilized to compute the expected substring failure density at the end of five years. Thus:

$$F_{SS} = 1 - (1 - 0.0005)^{2448} = 0.706$$

Using Figure 5, or by simply noting that the branch circuit and substring are one and the same, it is apparent that with only one cell failure per 10,000 per year, the array is more than 70% degraded after five years.

By way of contrast consider instead that the 144-cell module is reconfigured to consist of eight parallel cells by two series blocks with nine cells per substring, and one bypass diode per series block.

A branch circuit is now composed of $2448/18 = 136$ series modules and contains 272 series blocks. Using Equation 1 to compute the substring failure density gives:

$$F_{SS} = 1 - (1 - 0.0005)^9 = 0.00449$$

Entering Figure 5 with this substring failure density and interpolating for 272 series blocks indicates that the array degradation is now only about 2% after 5 years, a substantial improvement. Figure 6 expands on this result to illustrate the expected degradation in subsequent years and the result of different numbers of series blocks per branch circuit.

Module Yield Considerations

In addition to controlling array degradation, circuit redundancy features are also effective in improving module yield losses due to broken cells and other circuit failures which cause a module to be rejected during final assembly, shipping and installation. A common module failure criterion is based on controlling electrical mismatch in the array and stipulates that a module is rejected if its power loss is greater than 10% of the average peak power output for all modules. Figure 7 displays the dependence of module yield computed for this failure criterion as a function of module series/paralleling, for three sizes of modules, and for a cell failure density of one per thousand (10).

Considering the two 144-cell modules used in the previous example, Figure 7 gives a yield of 87% for the single-string module, and 99% for the module incorporating eight parallel cells by two series blocks.

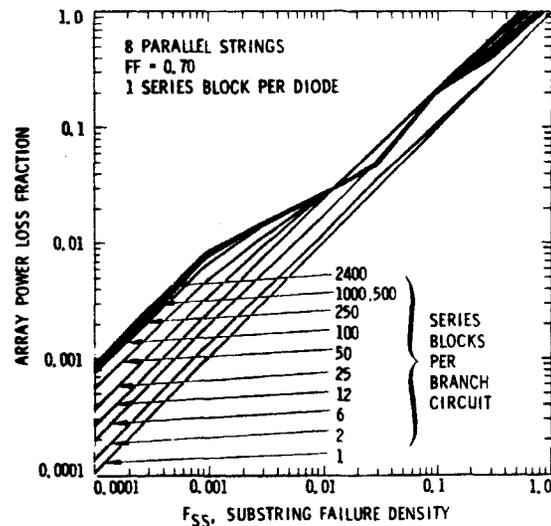


Figure 5. Array power loss as a function of substring failure density, for eight parallel strings, with one diode per series block

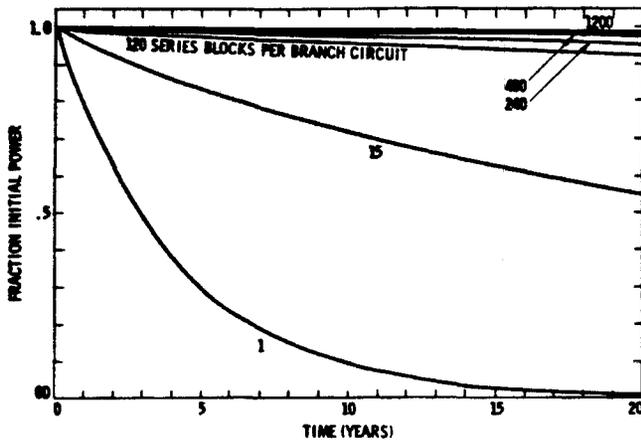


Figure 6. Array power degradation vs time for a constant yearly cell failure rate of 1/10,000, for eight parallel strings with bypass diodes

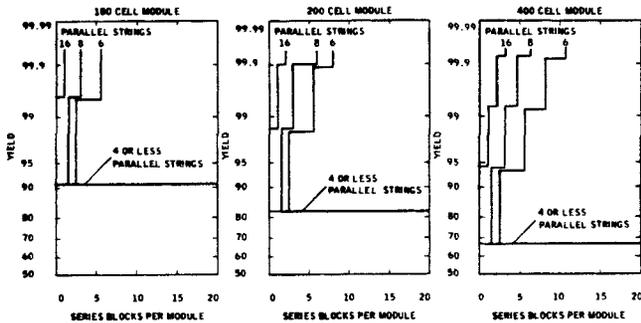


Figure 7. Module yield versus series paralleling assuming one failure per 1000 cells and module rejection for power loss greater than 10 percent

Hot-Spot Heating Considerations

A third subject related to array fault tolerance is consideration of the levels and effects of local cell hot-spot heating that can occur when a cell or group of cells is subjected to a current level greater than the cell's short-circuit current. As shown in Figure 8, this condition can be caused by a variety of circuit faults such as cell cracking, local shadowing, and open circuiting of series/parallel connections. When the degree of heating exceeds safe levels (100° to 120°C in most modules) the module's encapsulant system can suffer severe permanent damage (11). Such damage has occurred in a variety of present-day large application experiments and strongly suggests the use of bypass diodes or other corrective measures to limit the maximum heating level. References 10 and 11 describe means of determining the number of bypass diodes required and test methods to verify that hot-spot heating is limited to safe levels. For most cell and module constructions, a bypass diode is required around every 10 to 15 series cells.

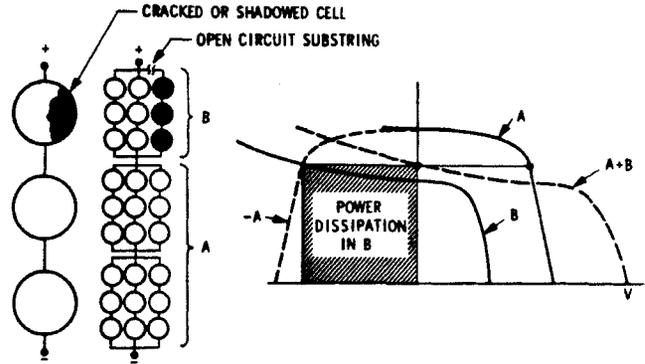


Figure 8. Visualization of hot-spot cell heating

COST-OPTIMUM REPLACEMENT STRATEGIES

Although it was shown in the previous section that circuit redundancy can substantially reduce array degradation associated with sporadic cell failures, module replacement is an additional strategy that can accomplish the same goal. One means of selecting the optimal maintenance/replacement strategy and level of circuit redundancy is based on minimizing the total life-cycle energy cost of a photovoltaic system over its design life. Following this author's previous work the optimization can be formulated by setting the life-cycle benefits equal to the life-cycle costs including module replacement (12, 13). The optimum system design is then found by minimizing the break-even cost of the photovoltaic energy which is given by:

$$R = \frac{C_0 + \sum_{i=1}^{20} C_i M_i (1+k)^{-i}}{\sum_{i=0}^{20} E_i (1+k)^{-i}} \quad (2)$$

where:

- R = Cost (worth) of energy (startup-year \$/kWh)
- E_i = Energy generated in year i (kWh)
- C_0 = Initial plant cost (startup-year \$)
- C_1 = Cost per module replacement action (startup-year \$/module)
- M_i = Number of modules replaced in year i
- k = Present value discount rate
- 20 = Plant lifetime (years)

Notice that the above expression allows a direct trade-off between the effects of array degradation versus time (E_i), the module initial cost (C_0), and the cost of module replacement ($C_1 M_i$).

To explore the general cost-effectiveness of module replacement it is instructive to apply the above methodology to the 1000-volt large ground-mounted array considered in the previous examples. If we assume typical array and balance-of-system costs and efficiencies per Ref. 13, and assume a cell failure rate of 0.0001 per year, we can calcu-

late the break-even life-cycle energy costs for various redundancy and replacement options using Equation 2. Figure 9 displays the calculated life-cycle energy costs for two replacement strategies as a function of the number of series blocks in branch circuits composed of eight parallel x 2448 series cells. In the first strategy no module replacement is allowed, and it can be seen that the life-cycle costs increase sharply with low numbers of series blocks. This reflects the rapid array degradation exhibited in Figure 6 for these circuit configurations. For the second curve in Figure 9 modules are replaced each time a solar cell fails during the 20-year life of the plant. This results in no power degradation, but does cause a substantial module replacement-cost contribution. This cost also varies with the number of series blocks due to reductions in module yield costs which occur when module series/paralleling achieves eight parallel by two or more series blocks. This degree of module series/paralleling is only possible in this example when 272 or more series blocks are used per branch circuit.

As seen in Figure 9 the optimum maintenance strategy depends on the degree of series/paralleling. When low degrees of series/paralleling are used, the least-cost maintenance strategy is to replace the affected module each time a solar cell fails. On the other hand, when a high degree of series/paralleling is used, the least-cost strategy involves no module replacement. Only in a very small region where the two curves cross is a partial-replacement strategy optimum. When considering Figure 9, it is apparent that the optimum configuration for an array of 4 ft by 4 ft modules in 8 parallel-string branch circuits is 272 or more series blocks, with no module replacement.

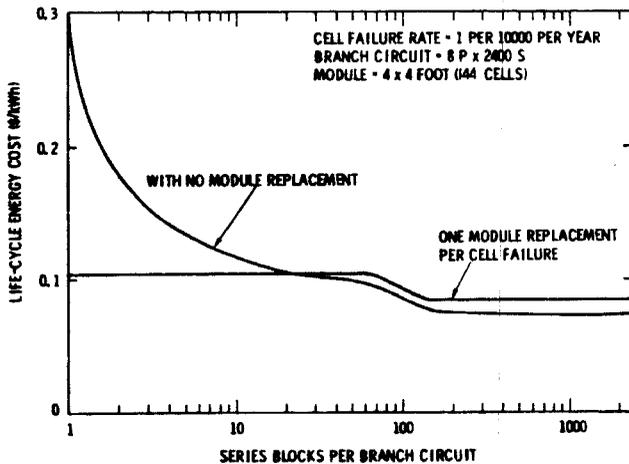


Figure 9. Life-cycle energy costs for 8 parallel-string branch circuits

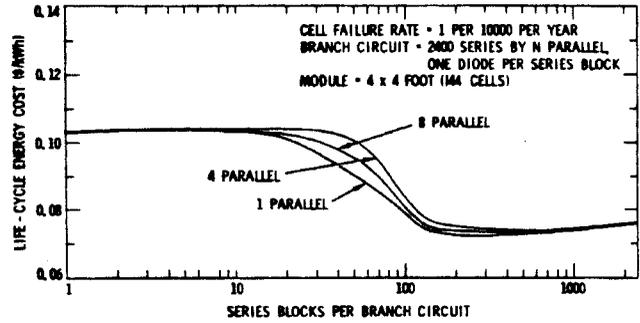


Figure 10. Minimum life-cycle energy cost with bypass diodes

Figure 10 expands the parametric study to include the effects of other choices for the number of parallel strings—in this case 1 and 4 strings in parallel. In this graph, only the optimum-maintenance (least life-cycle) cost is plotted for each number of series blocks per branch circuit. The number of parallel strings is found to have little influence on the overall conclusions relative to the optimum number of series blocks, or the optimum maintenance strategy.

CONCLUSIONS

It has been shown that cell failure rates as low as 0.0001 per year can significantly degrade array performance if appropriate circuit redundancy options are not applied. This high sensitivity to statistically extreme occurrences requires engineering design approaches based on statistical treatment of component endurance and operational stresses as opposed to more classical deterministic approaches based on mean values. Several statistical design approaches have been noted which address the areas of cell breakage, interconnect fatigue, glass breakage, and electrical insulation breakdown. The thesis of these methods is to quantitatively design for a specified low level of component failures, and then to control the degrading effects of the remaining failures through the use of fault-tolerant circuitry and module replacement. Means of selecting the cost-optimal level of component failures, circuit redundancy, and module replacement have also been described.

With today's component failure rates and with the use of multiple cell interconnects, series/paralleling and bypass diodes, it appears possible to achieve high levels of array reliability with no module replacement for routine component failures. The challenge of the future will be to maintain the present low component failure rates through diligent design, qualification testing, and field performance feedback.

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