TECHNOLOGY DEVELOPMENTS TOWARD 30-YEAR-LIFE OF PHOTOVOLTAIC MODULES

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ABSTRACT

As part of the United States National Photovoltaics Program, the Jet Propulsion Laboratory's Flat-Plate Solar Array Project (FSA) has maintained a comprehensive reliability and engineering sciences activity addressed toward understanding the reliability attributes of terrestrial flat-plate photovoltaic arrays and to deriving analysis and design tools necessary to achieve module designs with a 30-year useful life. The considerable progress to date stemming from the ongoing reliability research is discussed, and the major areas requiring continued research are highlighted. The result is an overview of the total array reliability problem and of available means of achieving high reliability at minimum cost.

INTRODUCTION

Over the past decade, research directed at improving the reliability of terrestrial photovoltaic modules has made substantial progress. From five-year-life modules of the early 1970's have come the 10-year to 20-year-life modules of today, and hopes for 30-year-life modules in the future. Research has been steady and productive; it has also concentrated on degradation mechanisms, such as cell breakage and interconnect fatigue, that are easily reproduced in short-term tests. Continued progress requires successful solutions for the more complex long-term degradation mechanisms that are difficult to measure accurately in the time available for laboratory research. These long-term mechanisms are expected to play an important role in the life-cycle economics of future large-scale power-generation applications.

Before assessing progress made by the Jet Propulsion Laboratory's Flat-Plate Solar Array Project toward long-life photovoltaic modules, it will be instructive to review briefly the key failure mechanisms identified to date, and target degradation levels for each that are consistent with a 30-year life. Because small levels of degradation or replacement are economically acceptable, a typical array meeting the target life will last somewhat longer than 30 years to recapture the life-cycle costs associated with the gradual degradation expected (see Figure 1).

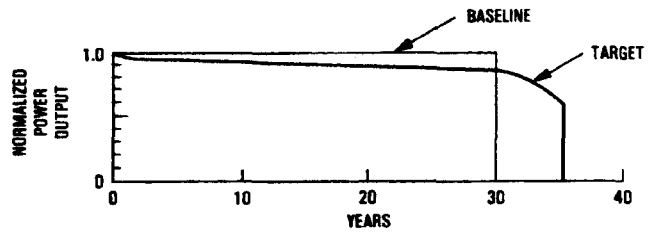

Figure 1. Typical Target Allocation for Time-Dependent Power Degradation

Table 1 lists 13 principal failure mechanisms, grouped into four types of degradation that reflect the general nature of the failures. The units of degradation listed in the third column provide a

Table 1. System Life-Cycle Energy Cost Impact and Allowable Degradation Levels for 13 Principal PV Module Failure Mechanisms

Type of Degradation	Failure Mechanism	Units of Degrad.	Level for 10% Energy Cost Increase*		Allocation for 30-year Life Module	Economic Penalty
			k = 0	k = 10		
Component failures	Open-circuit cracked cells	%/yr	0.08	0.13	0.005	Energy
	Short-circuit cells	%/yr	0.24	0.40	0.050	Energy
	Interconnect open circuits	%/yr²	0.05	0.25	0.001	Energy
Power degradation	Cell gradual power loss	%/yr	0.67	1.15	0.20	Energy
	Module optical degradation	%/yr	0.67	1.15	0.20	Energy
	Front surface soiling	%/yr	10	10	3	Energy
Module failures	Module glass breakage	%/yr	0.33	1.10	0.1	O&M
	Module open circuits	%/yr	0.33	1.10	0.1	O&M
	Module hot-spot failures	%/yr	0.33	1.10	0.1	O&M
	By-pass diode failures	%/yr	0.70	2.40	0.05	O&M
	Module shorts to ground	%/yr³	0.022	0.122	0.01	O&M
	Module delamination	%/yr³	0.022	0.122	0.01	O&M
Life-limiting wearout	Encapsulant failure due to loss of stabilizers	Years of life	27	20	35	End of life

*k = Discount rate

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convenient means of further quantifying the failure levels of the individual mechanisms according to their approximate time dependence. For example, units of %/yr in the context of component or module failures reflects a constant percentage of components failing each year. For components that fail with increasing rapidity, percent per year per year ($\%/y^2$) are the units used to indicate linearly increasing failure rate. This failure trend is most easily interpreted by noting that the failure rate after (A) years is (A) times the $\%/y^2$ value. For those mechanisms classified under power degradation, the %/yr units refer to the percentage of power reduction each year.

Using the units described above, columns 4 and 5 of Table 1 indicate the level of degradation for each mechanism that will result in a 10% increase in the cost of delivered energy from a large PV system. Because the mechanisms will generally occur concurrently, the total cost impact is the sum of the 13 cost contributions. Column 6 of the table carries the analysis a step further and suggests a strawman allocation of allowable degradation among the 13 mechanisms to achieve a total reliability performance consistent with expectations of a 30-year life. The total effect of the allowable levels is a 20% increase in the cost of energy over that from a perfect, failure-free system. The distribution among the mechanisms reflects this author's best judgment in light of likely achievable levels.

FAULT TOLERANCE AND REPLACEMENT STRATEGIES

In addition to improving the failure rates of critical components, two important additional strategies for reducing the overall reliability-related costs of a photovoltaic system are the introduction of fault tolerance into the array electrical circuit, and the implementation of an optimal maintenance strategy (1, 2).

It is important to note that the degradation levels presented in Table 1 assume the optimal use of fault tolerance within the array circuit and the optimal maintenance and replacement strategy. The last column of Table 1 indicates the choice of no maintenance, with decreased energy output as the penalty, or failed-part replacement, with increased operation and maintenance (O&M) costs as the penalty. The decision is driven by the cost of replacement versus the energy-loss increment associated with each component failure.

A key role of the electrical circuit of a photovoltaic array is reducing the energy impact of individual component failures such as cracked solar cells and fatigued interconnects. Figure 2 highlights those failure mechanisms that are affected, either positively or negatively, by the listed circuit features. Notice that the proper series-paralleling of the circuit requires a balance between enhancing the array's resistance to open-circuit and current-reduction mechanisms, and lowering the array's resistance to shorted cells and hot-spot heating. The use of bypass diodes, on the other hand, has a positive effect

Problems	Cell Paralleling	Contact Redundancy	Multiple Interconnects	Bypass Diodes	Cell Circuit Layout	Frequent Cross-Strapping	Ground-Fault Interrupt	Resistance Ground
Shadowed cells	+			+	+	+		
Interconnect fatigue	+		+	+		+		
Open-circuit cells	+	+		+		+		
Shorted cells	−					−		
Mismatched cells	+			+		+		
Ground-fault arc							+	+
In-circuit arcs	+	+	+	+				
Hot-spot heating	−			+		−		

Figure 2. Effect of Source-Circuit Features on System Energy Losses Caused by Various Failure Mechanism (+: lowered losses, −: increased losses)

in every case, but must be balanced against the cost of installing the diodes.

Figure 3 illustrates the general concept of series-paralleling and bypass diodes, and defines the nomenclature used to quantify various circuit configurations. The first step toward circuit redundancy is generally associated with dividing the large matrix of cells that makes up the array into a number of parallel solar-cell networks, referred to as source circuits. The individual source circuits provide convenient points for monitoring array performance, and provide an ability to isolate small areas of the total array for maintenance and repair.

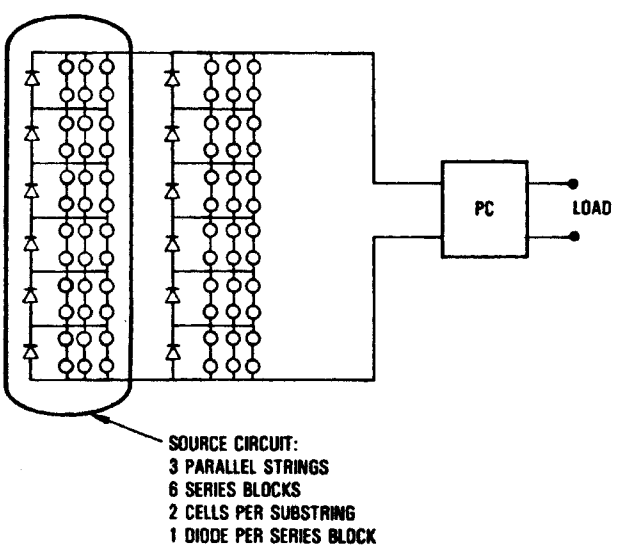


Figure 3. Series-Parallel Circuit Nomenclature

As shown in Figure 3, each source circuit may contain a single string of series solar cells or a number of parallel strings interconnected periodically by cross ties. The cross ties divide each source circuit into a number of series blocks. One

or more series blocks may also be bridged by a bypass diode, which is designed to carry the source-circuit current in the event that local failures constrict the current flow to the point of voltage reversal and power dissipation.

A key problem has been assessing the energy impact of sporadic component failures and quantifying the influence of specific series-parallel and bypass-diode arrangements. This problem has been solved for open-circuit failures by the development of an extensive parametric analysis based on the statistical distribution of failed substrings due to random cell open-circuit failures (3,4). Reference 4 contains a large number of parametric plots that allow rapid computation of the effects of cell failures and circuit redundancy on array power loss. An extension of this analysis is nearing completion for shorted cells by the authors. Figure 4 summarizes the results of this analysis for a 450-volt central-station source circuit and a failed-component fraction of 0.05% open-circuit cells and 0.05% short-circuit cells. It can be seen that the optimal tolerance to component failures exists with single-string source circuits with large numbers of bypass diodes.

Cells Per Substring	Series Blocks	Cells in Parallel				
		1	4	8	16	
20	50	0.001 0.011 0.012	0.001 0.050 0.051	0.001 0.025 0.026	0.001 0.015 0.016	
10	100	0.001 0.005 0.006	0.001 0.022 0.023	0.002 0.013 0.015	0.002 0.008 0.010	Optimum Design Region
5	200	0.001 0.003 0.004	0.002 0.010 0.012	0.002 0.007 0.009	0.002 0.004 0.006	
2	500	0.001 0.001 0.002	0.002 0.004 0.006	0.004 0.003 0.007	0.006 0.002 0.008	Sensitive to Shorted Cells

Top Line: Short-Circuit Losses
Mid Line: Open-Circuit Losses
Bottom Line: Total Losses

Figure 4. Fraction Power Loss Due to 0.05% Shorted Cells and 0.05% Open-Circuit Cells for a 450-volt (1000 series cell) Source Circuit Versus Series-Parallel Configuration, With One Bypass Diode per Series Block

Previous studies have further assessed the implications of these high degrees of circuit redundancy on module maintenance and replacement strategies (1). Figure 5 displays the relative life-cycle energy cost for two replacement strategies as a function of the number of series blocks and parallel cells per source circuit. In the first strategy (solid curves), no module replacement is allowed, and it can be seen that the life-cycle costs increase sharply with low numbers of series blocks. This reflects the rapid array degradation exhibited in Figure 4 in the same circumstances. For the second strategy (dashed curve) in Figure 5, modules are replaced each time a solar cell fails during the 30-year life of the plant. This results in no power degradation, but

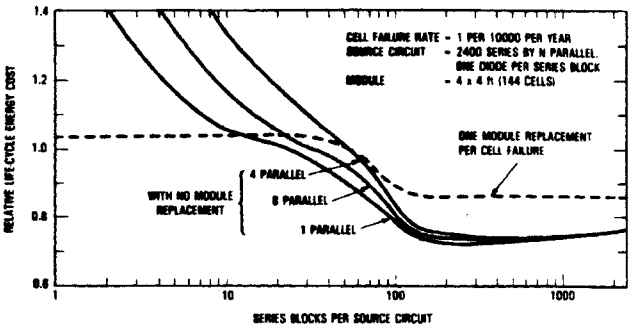


Figure 5. Relative Life-Cycle Energy Cost Versus Series-Paralleling and Maintenance Strategy

does cuase a substantial module replacement-cost contribution. This cost also varies with the number of series blocks due to improvements in module manufacturing yield that occur when module series-paralleling achieves high levels.

The key conclusion drawn from Figure 5 is that the optimal maintenance strategy is to not replace modules for routine sporadic cell failures, but instead to absorb the small economic penalty associated with the corresponding gradual decrease in plant power output.

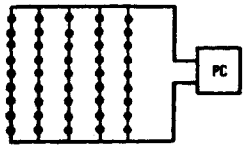
As noted above, the failure-rate data of Table 1 assumes the high level of redundancy and selective maintenance described. The critical question is therefore shifted to the feasibility of achieving the low failure rates indicated as being necessary in Table 1. The remainder of this paper examines our progress in this respect.

COMPONENT FAILURES

Component failures, for present purposes, are considered to be circuit elements such as solar cells and interconnects that may fail without requiring replacement of the total module. At the root of the high sensitivity to cell failures indicated in Table 1 is the need to interconnect large numbers of them in series to achieve the operating voltages of large applications. Figure 6 illustrates this sensitivity by noting the effect of one cell failure per 10,000 per year on system configurations that lack electrical redundancy. Even with the extensive redundancy recommended above, the sensitivity noted in Table 1 exists.

Cell Cracking

Of the cell-failure mechanisms seen in the field, cell cracking is probably the most prevalent. However, the number of cells with significant degradation (more than 25% degradation in short-circuit current) is very small, particularly with modern modules with high degrees of cell-contact redundancy. Most cracked cells remain electrically



ARRAY VOLTAGE	SERIES CELLS, S	POWER LOSS AT 5 YEARS, %
15	36	1.8
150	360	16.5
1500	3600	83.5

POWER LOSS = 1 - (1 - (YEARS x R))^S

Figure 6. Array Degradation for an Open-Circuit Cell Failure rate of 0.01% per Year Versus Number of Series-Connected Cells With no Circuit Redundancy

operative, because the cell metallization and cell interconnects bridge the break and complete the electrical circuit.

Quantification of cell failure rates requires extensive and expensive auditing of the actual field performance of multikilowatt photovoltaic applications. Past audits of early modules without modern contact redundancy, hail-impact resistance or resistance to hot-spot heating indicated cell failure rates due to cracking at between 0.1% and 0.02% per year (2). The primary causes of cell cracking in the early applications appeared to be differential expansion between the cell and its support, impact loading by hailstones, and reduced strength due to cell damage occurring during cell processing and module assembly. Qualitative design techniques have been developed addressing the first two causes (5,6), and cell proof-testing techniques can be used to screen out the one-out-of-a-thousand weak or damaged cell (7).

The introduction of glass superstrate modules has vastly reduced the incidence of differential expansion and hail-impact damage, and the introduction of multiple cell electrical contacts has similarly reduced the chance of a crack causing measurable electrical loss. Based on these improvements, it is estimated that current cell failure rates are on the order of 0.001% per year, and therefore easily consistent with the needs expressed in Table 1.

Shorted Cells

Historically, shorted cells have received little if any attention by the PV reliability research community. In small systems, sporadic short circuits lead to unmeasurable voltage losses with negligible energy consequences. However, as extensive cell paralleling is introduced into large central-station arrays, the sensitivity to shorted cells is substantially increased (see Figure 4). In addition, the emerging thin-film cells, such as those made of amorphous silicon, tend to fail shorted, and have increased our awareness of this failure mechanism. Even though they are hard to detect, shorted cells are fairly commonly encountered during the failure analysis of environmentally degraded single-crystal silicon modules. A common cause is the electrical interconnect shorting to the opposite junction of the cell as it leads from the bottom of one cell to the top of the next. Although no failure-rate data exist, the analyses behind Figure 4 suggest that the levels in Table 1 must be met. This is clearly an area requiring further study.

Cell Interconnects

Interconnect open-circuiting due to mechanical fatigue is a historical PV array failure mode that has been substantially eliminated in modern modules. Like cell breakage, it is primarily caused by thermal and humidity expansion differences between the cell and its supporting substrate or superstrate. Mon, Moore and Ross (8,9) have empirically characterized the fatigue-failure statistics of a variety of interconnect materials and geometries and have published detailed design methods for achieving optimal levels of interconnect reliability.

As with cell cracking, the solution is to design for very low numbers of failures (maybe 10% after 100 years) and then to incorporate interconnect redundancy to control power losses associated with those that fail.

From the empirical data, interconnects are found to fail with a log-normal distribution, with the weakest failing as much as 100 times sooner than the average. The low-probability tail of the distribution is well modeled as a linearly increasing failure rate. The levels indicated in Table 1 reflect easily achievable life-cycle optimums for doubly redundant interconnects, based on the work of the cited authors (9).

POWER DEGRADATION MECHANISMS

In addition to the component statistical failure mechanisms discussed above, a variety of observed mechanisms typically lead to gradual degradation or loss of power over the life of a PV array. These generally fall into two categories: optical losses and cell power degradation. Both of these degradation modes tend to be generic as opposed to being statistical; i.e., the majority of modules and cells of the same type degrade at the same rate with little statistical scatter. Most systems must be designed to accommodate this gradual power decrease, since the only correction techniques involve incremental addition of array area or total module replacement.

Gradual Power Loss in Cells

This category covers a variety of solar cell degradation mechanisms, including increased series resistance, junction shunting and deterioration of the cell antireflection (AR) coating. Increased series resistance is often associated with a gradual deterioration of the adherence between the cell metallization and the cell bulk material due to corrosion-related processes, or the deteriora-

tion of the ohmic contact through the formation of a Schottky barrier. Junction shunting, which is much less common, may be caused by the diffusion or migration of metallization elements into the cell juction or over the external surfaces of the cell. The third cell degradation mechanism relates to the deterioration of the AR coating on the solar cell's irradiated surface due to leaching or contamination from plating or corrosion products. All of these mechanisms lead to a gradual reduction in the cells electrical efficiency and are quite sensitive to the choice of metallization and AR coating materials and processes. Work at Clemson University has shown that moisture and thermal aging are key environmental stresses, and that the module encapsulant system exacerbates the problem as often as it helps (10, 11).

In all three mechanisms, the most effective techniques for quantifying expected levels of degradation involve accelerated temperature/humidity testing together with Arrhenius plotting and other means of relating the data to long-term use conditions (10, 12, 13). Application of these techniques to present commercial modules suggests that the 0.2% per year drop of power assumed in Table 1 should be achievable with future low-cost concepts.

Module Optical Degradation

Aside from external surface soiling, discussed in the next subsection, module optical degradation is generally caused by encapsulant transmission loss in the form of uniform yellowing due to ultraviolet (UV) and temperature-induced self-degradation, or local yellowing due to foreign matter diffusing into the encapsulant: e.g., from edge seals, mounting hardware, and electrical-terminal hardware.

Substantial research has been done on these various degradation mechanisms over the past few years, and a variety of highly stable materials and additives have been identified (5, 14). Of key importance, in addition to starting with UV-resistant materials, is the proper incorporation of UV absorbers and antioxidants, and preventing their loss over time due to leaching and diffusion. Similarly, interfacing materials such as gaskets and electrical terminal hardware must be carefully chosen for chemical compatibility with the primary cell encapsulant.

As with the cell degradation mechanisms, the most effective techniques for quantifying expected levels of degradation involve carefully accelerated temperature/humidity and UV testing, together with various means of relating the data to long-term use conditions (12, 13, 14). A key factor in such testing is properly accelerating the mechanisms that cause loss of the stabilizing additives. Vented ovens and water sprays play an important role in this respect.

With modern encapsulants, such as highly stabilized ethylene vinyl acetate (EVA), proper choice of interfacing materials, and careful attention to preventing loss of the additives, it is expected that the 0.2% per year degradation rate listed in Table 1 is achievable.

Front-Surface Soiling

Although similar in effect to other optical-loss mechanisms, experimental data indicate that optical surface soiling due to dust and atmospheric contaminants reaches equilibrium levels in a few weeks and then fluctuates somewhat with natural cleaning mechanisms such as rain. The net result is most easily modeled as a fixed loss in array current and power over the life of the array.

Figure 7 illustrates this soiling behavior for a variety of module surface materials in two site environments--one urban, the other remote. These and other data gathered by JPL over the past six years at a variety of sites in the United States indicate that average soiling levels below 5% should be easily achievable with glass or Tedlar-like optical-surface materials, without washing (15). Very dusty remote sites and heavily polluted urban sites will, of course, exceed these levels, and may require periodic washing.

In response to these data, Table 1 suggests a 3% allocation for fixed soiling-related losses.

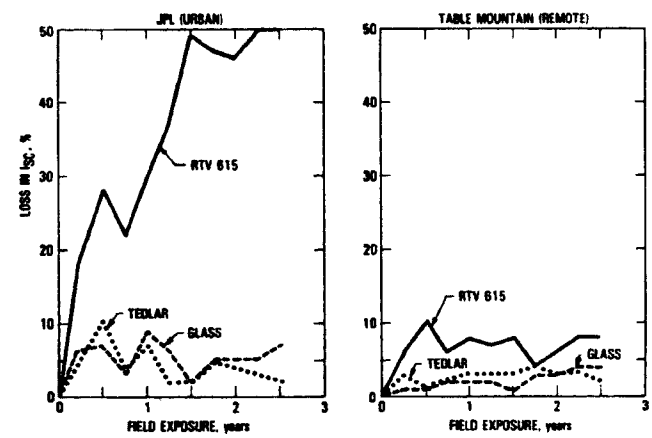


Figure 7. Loss in Array Short-Circuit Current (I_{SC}) Due to Soiling Versus Days of Field Exposure

MODULE-FAILURE MECHANISMS

In addition to component failures that are best treated at the cell level, a number of failures are more appropriately considered at the module level. These include glass breakage, electrical insulation breakdown, and various types of major encapsulant failure such as delamination. Like cell failures, these failures are also flaw-related and must be treated statistically when considering quantities of modules in a large array.

When designing for appropriate levels of module failures, it is important to note that a module failure is likely to cause an electrical hazard or major power loss and will therefore require immediate repair or replacement. As a result, module failure rates are traded off against life-cycle maintenance costs as opposed to redundancy and life-cycle energy loss, which are associated with cell failures.

Module Glass Breakage

With the extensive development of glass superstrate modules in recent years, many of the reliability problems of past module designs have been substantially solved. At the same time, however, glass breakage was introduced as a possible failure mechanism. Although vandalism is probably responsible for some glass breakage, other key causes include frame-induced thermal stresses, handling damage, wind loads, and hail impact.

Thermal-stress failures are generally caused by mounting untempered glass in a frame, which leads to the periphery of the glass heating more slowly than the center area when sunlight strikes the dark, absorbent solar cells. The expanding center places the flawed glass edges in tension, leading to mechanical stresses greater than that allowable for untempered glass. With its increased strength, tempered glass is easily able to withstand the thermal stresses, and provides an effective solution to the problem.

Substantial research has been conducted over the past few years to develop means of accurately predicting the breaking strength of glass subject to uniform pressure loads. Because glass fracture is dependent on the coincidence of a flaw and a high stress, glass strength varies widely from sheet to sheet and from location to location within a sheet. Based on a combination of nonlinear stress analysis and empirical fracture data, Moore provides a convenient tool for sizing glass for a given probability of failure due to uniform pressure loads such as wind and snow (16). In a second document he also describes a useful cyclic loading test technique (17). For design purposes, a uniform loading of 50 lb/ft^2 is commonly used because it provides a low probability of being exceeded and has a minimal effect on module price.

Design and test techniques for hail-impact loading have also been developed in response to high levels of field failures with nonglass modules due to hail impact (6, 18, 19). Field experience indicates that resistance to 1-in.-dia hail is required, even in low-hail-incidence regions of the country. This large size reflects the design margin required to achieve the low probabilities of failure outlined in Table 1.

Module Open Circuits

Module open-circuiting is the result of a major break in the module electrical circuit, generally involving the bus wiring or output connection. Although no quantitative statistical data have been gathered to this author's knowledge, such failures have been encountered at JPL with modest frequency during the failure analysis of field problems. Thermal differential expansion stresses and poor solder joints are the cause of many of the observed failures. It is expected that attention to these issues, together with careful qualification testing, will allow the levels in Table 1 to be achieved.

Module Hot-Spot Failures

A third cause of module failures is excessive local cell hot-spot heating that can occur when a cell or group of cells is subjected to a current level greater than the cell's short-circuit current. As shown in Figure 8, this condition can be caused by a variety of circuit faults such as cell cracking, local shadowing, and open-circuiting of series/parallel connections. When the degree of heating exceeds safe levels (100° to 120°C in

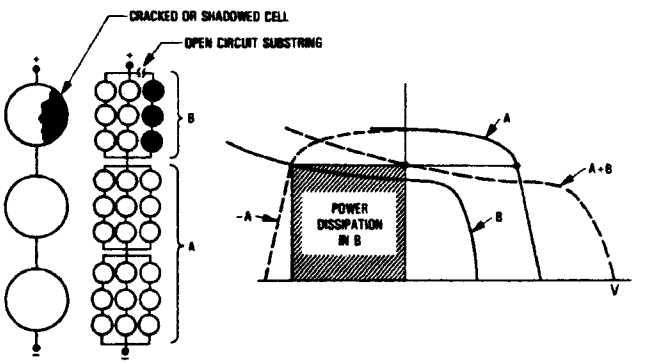


Figure 8. Visualization of Hot-Spot Cell Heating

most modules) the module's encapsulant system can suffer severe permanent damage (20). Preventing such damage requires the use of bypass diodes or other corrective measures to limit the maximum heating level. References 4, 19, 20, and 21 describe means of determining the number of bypass diodes required and test methods to verify that hot-spot heating is limited to safe levels. For most cell and module constructions, a bypass diode is required around every 10 to 15 series cells.

Failed Bypass Diodes

Although bypass diodes represent an important means of improving array reliability, at the same time they introduce additional failure mechanisms.

Like module open circuits, instances of internally shorted bypass diodes and diode shorts to ground have been observed, but not quantified. Recent work on diode reliability indicates that very little historical data are applicable to the PV module bypass application, which involves long periods of low (5-volt) reverse voltage together with periodic high forward currents. Because diode junction temperature is the critical factor related to long-term reliability, it is recommended that the junction temperature of silicon diodes be

maintained below 125°C under conditions of maximum bypass current and ambient temperature (22). Assuming proper heat-sink design, historical diode reliability data are entirely consistent with the values allocated in Table 1.

Module Shorts to Ground

An important module failure mechanism from a safety point of view is breakdown of the electrical insulation system between the cell circuit and grounded module exterior surfaces. The maximum voltage stress includes consideration of maximum open-circuit array voltages achieved under low temperature (0°C) and high irradiance (100 mW/cm^2), as well as transient overvoltages due to, for example, system feedback of lightning transients. The latter is bounded by the characteristics of incorporated voltage-limiting devices such as MOVs.

Because voltage breakdown tends to occur at insulation flaws and sites of stress concentration, voltage withstand level is found to vary widely from module to module (23). Screening out of manufacturing defects is usually accomplished by testing each module at a hi-pot voltage level of twice the worst-case system voltage plus 1000 volts. Passing this hi-pot test is the key module requirement on initial voltage-withstand performance.

A second important requirement is the limiting of array leakage currents under normal operating conditions. This requirement is driven by the demands of array ground-fault detection systems, which require that normal leakage-current levels be below the threshold trip level set to note a voltage breakdown. The required leakage level is a function of the number of modules per detection system and the system operating voltage.

Long-term field performance must additionally include the expected degradation of the insulation materials and construction through the action of weathering and voltage-stress exposure. Delamination, cracking and electrochemical corrosion are important degradation mechanisms.

Electrochemical corrosion is caused by array leakage currents that lead to the migration of corrosion products between the solar cells and the module frame. With time, the products bridge the insulation with a conductive path that results in a short to the grounded module frame. Mon et al (24) point out that the level of corrosion is proportional to the total integrated ionic leakage current (amp-hours) as influenced by module temperature and humidity conditions; electronic leakage current associated with the conduction of electrons does not lead to corrosion.

Because ground-fault failures generally require immediate repair and often lead to plant shutdown, very low failure levels are required. For modules where breakdown is largely constrained to occur between the cell circuit and the module's peripheral frame, it is useful to address the allowable number of breakdowns per year per mile of module periphery. Table 1 assumes a linearly increasing rate of failures over the plant's life based on historical experience with voltage breakdown and the accrued damage characteristics of electrochemical corrosion. The indicated value of $0.01\%/y^2$ corresponds to a failure rate of 0.1%/yr (or one breakdown per 3 miles of module periphery per year) after 10 years.

Prediction of voltage breakdown reliability is very poorly defined and requires substantial research.

Module Delamination Failures

Delamination of the module encapsulant system is another historical failure mode for terrestrial modules. It is heavily influenced by the choice of materials and processes. Although module designs of the mid-1970's often experienced high failure rates due to this mechanism, recent development of improved interface primers and laminating procedures has drastically reduced instances of early delamination in the field. Coulter et al (25) summarize the state of the art of module bonding technology and list effective interface primers for use in various module encapsulation systems. The art of life prediction or failure-rate prediction, on the other hand, is not well developed for the mechanisms associated with debonding. A significant contributing factor is the number and complexity of mechanisms involved. These involve processing sensitivities such as cleanliness and primer thickness, environmental reductions in bond strength due to moisture and photothermal aging effects, and increased module stresses due to material shrinkages and differential thermal and humidity expansion.

Table 1 assumes that we can eliminate the generic delaminations encountered in the past, and reduce the problem to one of processing-induced random failures that increase over time due to environmental aging effects. Significant research is still required to relate where we are, quantitatively, to the economic requirements of Table 1.

LIFE-LIMITING WEAROUT MECHANISMS

The last degradation category is the most difficult to quantify through known failure mechanisms. Most of the known mechanisms have been studied and found to be gradual or statistical in nature and not associated with a wear-out end of life such as might be associated with automobile tires or light bulbs.

Mechanical fatigue of cell interconnects is a classic example of a wearout mechanism. However, to achieve the desired low rate of random interconnect failures during the early life of the array, the wearout life associated with 10% failures will typically be more than 100 years.

Encapsulant failure due to depletion of UV absorbers and voltage breakdown due to electrochemical treeing are two mechanisms recently found to display life-limiting failure trends. With UV absorbers and other encapsulant stabilizers there

may be little degradation while the additives are slowly depleting over time. However, once the concentrations drop below critical levels, the encapsulant rapidly degrades.

Electrochemical-corrosion-induced voltage breakdown is similar to mechanical fatigue in that it is a mechanism associated with accrued damage. In this case the relevant measure is total amp-hours of electrical charge transfered in the corrosion path.

With both mechanisms it is not clear whether random failures due to processing variations or generic wearout will govern. As a result, both mechanisms were also discussed above, under the category of module failures. From an end-of-life point of view it is important that the annual cost of maintenance and replacement stay well below the annual worth of electricity produced, until after 30 years.

SUMMARY REMARKS

Achieving 30-year life flat-plate PV modules requires a systematic approach to the identification of failure mechanisms, to the establishment of allowable failure levels, and to the development of cost-effective solutions. Table 1 provides updated targets for allowable failure rates based on the life-cycle-cost requirements of future large-scale applications and the technical realities of available PV materials and processes. These future requirements were compared with the present performance and our state of knowledge with respect to 13 principal mechanisms. Achieving 30-year-life modules requires that each mechanism be understood and that design and test approaches be available. Figure 9 summarizes this status in pictorial form to provide a quick reference to past areas of success and to those areas requiring continued research. A quick glance indicates substantial progress to date, but also the need for much additional research.

Degradation Mechanism	Problem Level Understood	Parameter Dependencies Quantified	Qual Test Available	Quantitative Life Tests Available	System Impact Quantified	Cost-Effective Circuit Redundancy Defined	Cost-Effective Failure Level Achieved
Open-circuit cracked cells	◐	◐	●	○	●	●	●
Short-circuit cells	○	○	●	○	◐	◐	Unknown
Interconnect open circuits	●	●	●	●	●	●	●
Cell gradual power degrad.	◐	◐	●	●	●	◐	●
Module optical degradation	◐	◐	◐	◐	●	◐	◐
Front-surface soiling	●	◐	○	○	●	NA	●
Module glass breakage	◐	●	◐	○	●	NA	Unknown
Module open circuits	◐	○	●	○	●	◐	Unknown
Module hot-spot failures	◐	●	●	○	○	◐	◐
Shorted bypass diodes	○	◐	◐	○	●	◐	Unknown
Module shorts to ground	○	◐	○	◐	●	◐	Unknown
Module delamination	◐	◐	◐	○	◐	NA	Unknown
Life-limiting wearout	○	○	○	○	◐	NA	Unknown

●: Substantially Complete ◐: Partially Complete ○: Substantially Incomplete

Figure 9. Status of Research on 13 Principal Flat-Flat-Plate Array Degradation Mechanisms Using Crystalline Silicon Solar Cells

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