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Design of Fault-Tolerant Circuits for Photovoltaic Concentrators

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ABSTRACT

A methodology for fault-tolerant design of photovoltaic concentrator module and array circuitry is presented. Results are provided in the form of example analyses and a complete set of curves giving array power loss versus fraction of open-circuit failures for a broad variety of series-parallel configurations with bypass diodes. Specific curves are provided for single, four, eight, and sixteen-parallel-string source circuits with varying bypass diode frequencies. A example case is presented in a step-by-step fashion to assist the module or array designer in using the above mentioned curves to calculate expected power loss for other concentrator designs. Optimum circuit configurations must also reflect the costs of incorporating circuit redundancy features and the life-cycle tradeoffs associated with repair and replacement of failed modules. To this end, module replacement strategies are also investigated based on a set of projected module and array costs. The results highlight circuit design configurations and module replacement strategies that maximize the array benefit to cost ratio.

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GLOSSARY

Array	A mechanical assemblage of modules and a sun-tracking mechanism in a common support structure.
Array field	An assemblage of arrays connected electrically in series and/or parallel to one or more power converters.
Array-field power-loss fraction	The power loss suffered by an array field as a fraction of the initial undegraded array-field power (measured at some standard test condition).
Back-bias voltage	Voltage applied across a cell in the negative polarity.
Bypass diode	A diode that is connected in parallel with a group of series cells (or parallel strings of series cells) so that it conducts only when the voltage across the cells is in the reverse polarity.
Cell failure fraction (density)	The fraction of all cells in an array that have failed open-circuit.
Cell failure rate	The fraction of cells failing per given time unit, usually a year.
Concentrator module	An environmentally protected package of solar cells complete with concentrating optics.
FF	Fill factor (see below).
Fill factor	A parameter used to quantify the shape of a current-voltage (IV) curve of a photovoltaic element (cell, module, array, etc.); the value is defined mathematically as the maximum power out of the element divided by the product of its short-circuit current and open-circuit voltage (i.e., $P_{max}/(I_{sc} \times V_{oc})$).
Life-cycle benefit	The total present value (dollars) of the energy generated by an array over its defined lifetime.
Life-cycle cost	The total present value of all invested cost in a system over its defined lifetime--used in a limited sense in this report to include initial system cost (including bypass diodes) and module replacement cost.

Reverse quadrant	Refers to the current-voltage characteristics of a solar cell in the range where current is flowing in the positive direction, but where the voltage across the cell is negative, or reversed.
Reverse voltage	See back-bias voltage.
Series block	A collection of one or more cell substrings wired in parallel.
Series blocks per diode	The number of Series Blocks connected in series between the attachment points of each bypass diode.
Series blocks per source circuit	The total number of Series Blocks connected in series in a Source Circuit.
Source circuit	A network of solar cells interconnected in series and parallel so as to develop full system voltage.
Substring of cells	A small group of cells wired in series.
Substring failure field fraction (density)	The fraction of all substrings in an array-containing one or more open-circuit cells.

SECTION I

INTRODUCTION

A. REPORT OBJECTIVE AND ORGANIZATION

An important module and array system performance criterion is fault tolerance. Because enhancing fault tolerance through initial module and array design can prove to be more cost effective than module replacement later, a key objective of this report is to develop a methodology and to present analytical results that will allow the concentrator module designer to achieve cost-optimum levels of circuit fault tolerance.

Because module replacement and maintenance are integral parts of achieving minimal life-cycle costs, maintenance and replacement tradeoffs were also conducted to understand their influence on optimal circuit design strategies. The results were generated and are presented parametrically to allow their application to a broad variety of concentrator module and array designs with differing economic assumptions and with various achieved piece-part failure rates.

Because of the statistically low number of piece-part failures expected, a significant fraction of this report is devoted to the problem of computing the system power reduction associated with infrequent random cell open-circuit failures in complex series-parallel circuits with and without bypass diodes. The detailed methodology is presented in Appendix A and is reduced to 24 parametric plots that are contained in Appendix B.

Section II, immediately following this section, summarizes the overall methodology for computing the fault tolerance of various source-circuit configurations. An example system design problem is introduced as a means of exploring and illuminating the key circuit design tradeoffs and issues in achieving different levels of fault tolerance.

To arrive at optimal levels of fault tolerance one must include the economic implications of implementing the circuit redundancy features and include the economic tradeoffs associated with optimal maintenance and/or replacement of failed modules. These considerations are discussed in Section III and are illustrated for two sets of system design and economic assumptions. One set of assumptions was chosen to be representative of present-day economics and technology; the other is more representative of long-range goals.

Section IV draws conclusions which, of course, must be interpreted in the light of the assumptions made in the examples. Although the examples were chosen to be as relevant as possible to present-day issues, the report contains the means to allow the reader to readily repeat the analyses using differing assumptions.

B. CONCENTRATOR ARRAY NOMENCLATURE

Before embarking on a discussion of fault tolerance, we need to consider the nomenclature associated with modules, arrays and array fields. First, it is important to note that the electrical-circuit modularity of a large photovoltaic (PV) array field is generally not the same as its mechanical modularity. Thus two sets of modular-element definitions have evolved--those associated with the mechanical system (module, array), and those associated with the electrical circuitry (substring, series block, source circuit). Because both sets of elements are built up of aggregations of solar cells, each places constraints and requirements on the other.

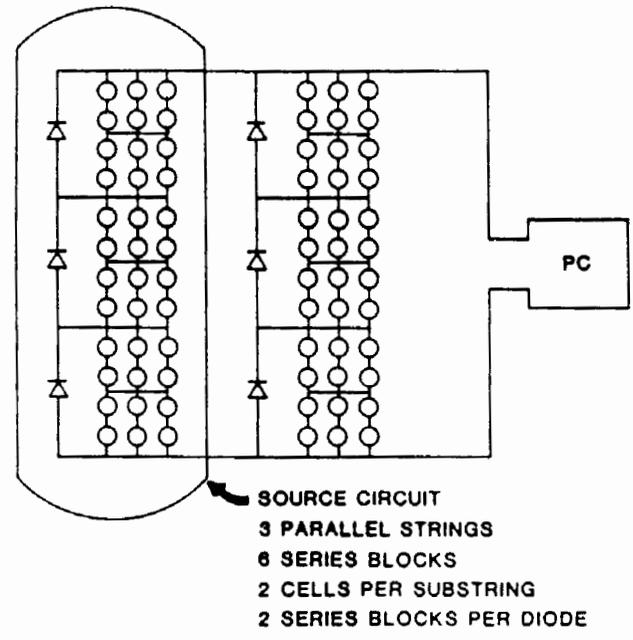
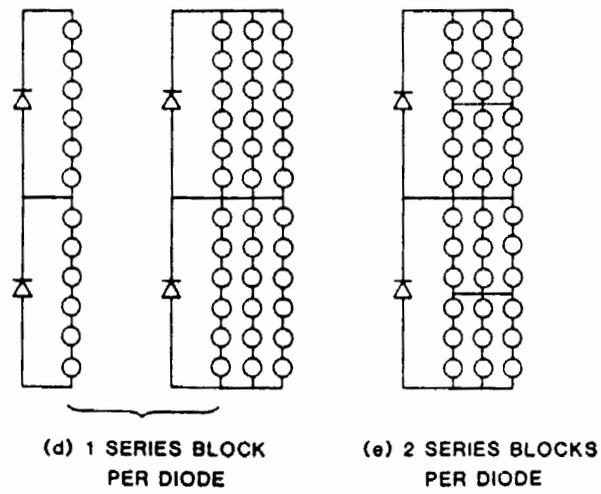
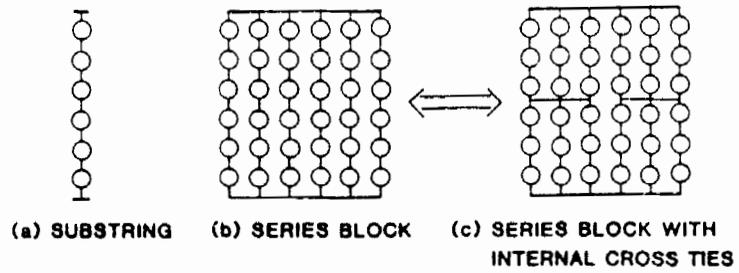
Starting with the mechanical elements, a photovoltaic concentrator module consists of an environmentally protected package of solar cells complete with concentrating optics. It is the equivalent of a circuit board in a computer or television. An array is a mechanical assemblage of modules and a sun-tracking mechanism in a common support structure. The array is therefore somewhat analogous to an electronic chassis--a mechanical integration of circuit boards. When a number of arrays are combined in a large application, the collection of arrays is referred to as the array field.

Although modules and arrays house portions of the electrical circuit of the array field, the fundamental building blocks of the electrical circuit generally do not coincide with the mechanical building blocks. Thus a separate system of electrical circuit nomenclature has developed as noted in Figure 1.

The lowest level building block is a cell-substring which is a collection of series cells (Figure 1a). Next in complexity is a collection of one or more substrings in parallel termed a series block (Figure 1b). The analytical model, used to obtain array-power-loss fraction and described in detail in Appendix A, does not deal directly with series blocks having internal cross ties as shown in Figure 1c. However, for practical systems with low cell failure densities, i.e., one or fewer failures per series block, the internal cross ties can be ignored with great accuracy, and a configuration such as Figure 1c can be approximated by one such as Figure 1b.

Bypass diodes are normally included to improve fault tolerance and prevent damage due to hot-spot heating. Each bypass diode is connected in parallel with one or more series blocks (Figure 1d-e). The number of series blocks per diode is an important parameter used in the analyses described here.

A source circuit consists of a series interconnection of series blocks, including bypass diodes, configured to reach full system voltage (Figure 1f). Generally a source circuit will coincide with an integral number (1 or more) of series-connected arrays.



(f) ARRAY FIELD WITH 2 SOURCE CIRCUITS

Figure 1. Module and Array Electrical Circuit Nomenclature

Finally at the system level, the total array field is made up of paralleled source circuits as shown in Figure 1f. Although the figure only shows two source circuits, an array field will generally be made up of a large number of source circuits, from ten to as many as a few hundred.

The series-block and substring elements of the source circuit are mechanically housed in individual modules. Usually a module will be designed to represent an integral number of substrings or series blocks to simplify the circuit wiring at the array level. It is the goal of the module designer to achieve a module that can be economically integrated into an array source circuit that contains the required series-parallel and fault-tolerance features.

C. FAULT-TOLERANCE STRATEGIES

Two important circuit design strategies are considered in this report for the purpose of enhancing fault tolerance. The first is the use of increasing numbers of series blocks and parallel strings per source circuit. This is accomplished by increasing the numbers of cross-connections between the parallel strings of cells; these cross-connections are called cross-ties.

The objective of this cell paralleling is to provide alternate circuit paths to carry the source-circuit current under conditions where the current output from a localized number of cells falls below that of the overall source circuit. Such local current-output reductions can result from a number of causes such as open circuiting of individual cell interconnects and solder joints, loss of cell area from breakage, or partial shadowing due to localized obstructions or soiling. Unfortunately, the level of over-current that can be absorbed by the parallel cells is limited by their short-circuit current. When their short-circuit current limit, which may be only 10 to 20% above their operating current, is reached, the entire group of parallel cells becomes reverse-biased and begins to dissipate power. This power dissipation heats the cells and can cause severe cell and module physical degradation. The result is referred to as hot-spot heating from the fact that the cells do not heat uniformly, but instead develop local hot-spots. This implies that the use of cell paralleling to increase fault tolerance requires a significant degree of paralleling.

The second fault-tolerance strategy, which addresses the hot-spot heating problem, is the use of bypass diodes. Bypass diodes are installed in parallel with groups of solar cells, as shown in Figure 1, so as to limit the maximum levels of voltage reversal and power dissipation within the bypassed cells. Under conditions of localized current reduction, a bypass diode carries the over current and prevents the entire group of cells from going into a state of severe voltage reversal and power dissipation. However, even with a bypass diode, individual cells can be exposed to reversed voltages and heating equal to the sum of the voltages and powers, respectively, generated by the good cells in the bypassed group. The number of cells per bypass diode, particularly the number of series cells per diode, is therefore an important parameter for controlling maximum hot-spot heating levels. Although the exact number depends on the thermal design and

heating endurance of a particular concentrator, the maximum acceptable number of series cells per bypass diode is generally in the range of 5 to 10.

For a detailed discussion of hot-spot design and test methods for concentrator photovoltaic modules, the reader is referred to previous work (References 1 and 2).

SECTION II

CIRCUIT OPTIMIZATION METHODOLOGY

Each circuit design strategy has advantages and disadvantages. The optimal strategy generally involves a tradeoff of the cost of implementing the technique versus the gain in performance and reliability. To ascertain the effectiveness of various degrees of series-paralleling, the power output of an array under specific failure conditions must be determined for a variety of series-parallel configurations with varying numbers of bypass diodes. Power loss varies inversely with degree of series-paralleling, but limits imposed by physical constraints, as well as those of cost, make it impossible to achieve negligible power loss by means of unlimited series-paralleling. Thus a number of configurations offering acceptable power loss must be considered.

In the analyses described in this report, only open-circuit failures are considered. The analysis of the effects of failures on a large array field requires a complex statistical approach; in order to make the analysis manageable, only the statistics of the occurrence of open-circuit failures was considered. This neglecting of shorted cells is well justified for single-string photovoltaic concentrator arrays, because infrequent shorted cells simply cause a small voltage loss, proportional to the fraction of failed cells. Only in the case of large numbers of parallel cells and series blocks per source circuit does one need to be sensitive to magnifying the impact of infrequently occurring shorted cells. In the limiting case of a cross-tie after each group of n parallel cells, the power loss due to shorts is simply n times the loss in single-string source circuits. See Reference 3 for a more detailed discussion of the impact of shorted cells.

For the case of one cell per substring, the results of the analysis for open cells become applicable to an array with partially failed cells: e.g., a series block of eight parallel substrings with one failed open can be used to simulate one of four parallel substrings and one cell 50% degraded.

A. ARRAY POWER LOSS CALCULATION

In the analysis described here array power loss is calculated as a function of the array circuit parameters using the analytical approach presented in Appendix A. In summary, the first step is the use of the binomial distribution, starting with an assumed fraction of cell failures, to predict for each source circuit, the fraction of series blocks in the source circuit having various numbers of failed substrings. The second step involves the generation of I-V curves representing the degraded source circuits. Specifically, the I-V curves of a series block containing one or more open-circuit substrings are determined and then combined to predict the performance of source circuits containing the distributions of degraded series blocks determined by use of the binomial theorem as discussed above.

Finally, the system power loss is computed based on the predicted fraction of source circuits that contain each distribution of degraded series blocks. The actual power loss determination is made by adding the degraded source-circuit I-V curves in parallel and comparing the resultant power with that for the same system without any failed cells.

The process as described above is quite complex and requires a combination of extensive statistical computations, precision I-V curve additions, and graphical interpolation. To allow module and array designers to compute the power loss associated with various series-parallel diode systems, the results of the above methodology have been reduced to an extensive series of parametric plots located in Appendix B. An example plot for single-string source circuits is reproduced in Figure 2. This figure provides the predicted fraction array power loss (on the abscissa) for any given fraction of failed substrings in the array (F_{SS}) (on the ordinate), with number of series blocks per source circuit as a parameter.

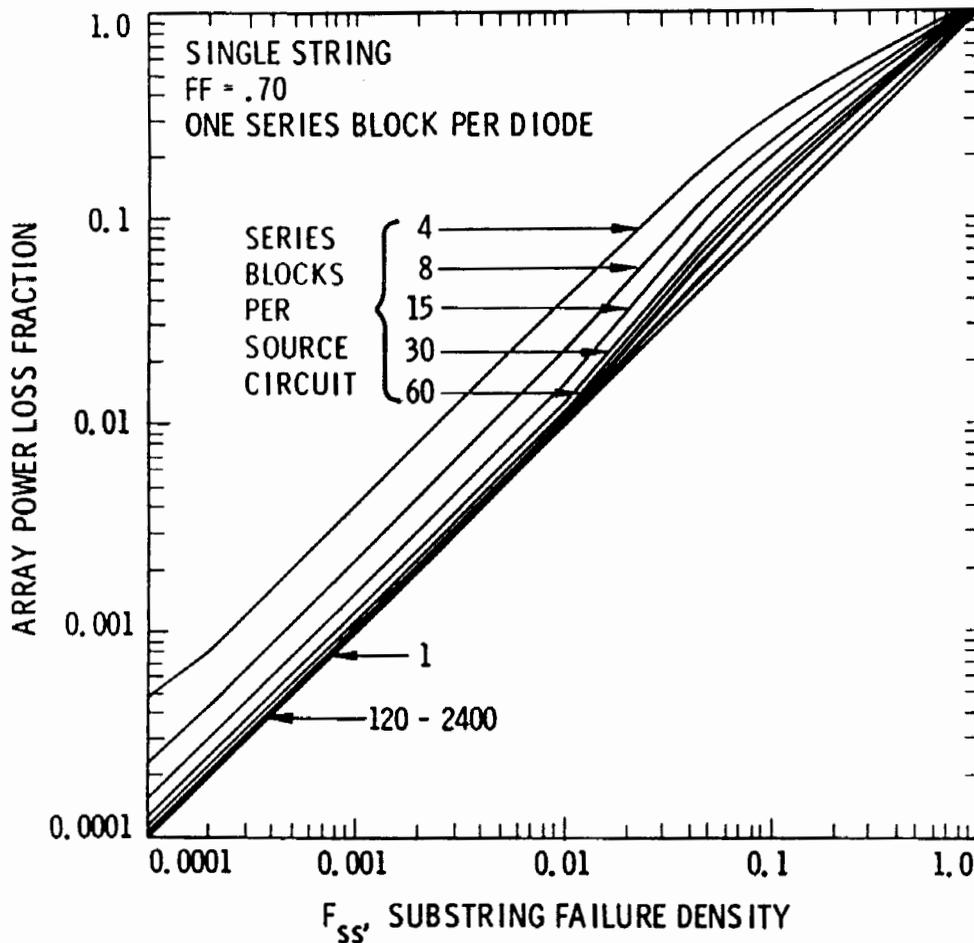


Figure 2. Array Power-Loss Fraction vs. Substring Failure Density for a Single-String Source Circuit with One Series Block per Diode

In this case of a single series string, the number of series blocks is defined by (equals) the number of bypass diodes per source circuit. In the more general case with paralleled cells, the number of series blocks is determined by the number of cross-ties; the bypass diodes may then be installed in parallel with one or more series blocks. Curves are provided in Appendix B for 4-parallel, 8-parallel and 16-parallel source circuits with a variety of bypass diode frequencies. The curves were used to determine array power loss in all of the calculations described in this report. The set of curves is complete enough to encompass most array circuit configurations, for both large and small systems, and provides a useful tool for analysts performing studies of the type discussed here. A broad variety of systems can be analyzed by interpolating among the various graphs, and among the curves on each graph.

To use the curves one must first compute the fraction (F_{SS}) of open circuit substrings in the array field corresponding to some predetermined or assumed fraction of open-circuit solar cells. Statistically this is the fraction of substrings containing one or more failed cells and is given by the following equation:

$$F_{SS} = 1 - (1 - F_C)^{N_C} \quad (1)$$

where:

F_{SS} is the substring failure fraction
 F_C is the cell failure fraction
 N_C is the number of cells per substring

Equation 1 is derived from the binomial-distribution equation (Equation A-1 in Appendix A); the latter equation gives the probability of obtaining x failures out of N trials. The second half of the right side of Equation 1 is the probability of obtaining no cell failures in any particular substring of N_C cells, where the probability of any given cell being failed is F_C . The probability of having one or more cell failures in the substring is 1 minus the probability of no cell failures.

B. FAULT TOLERANCE OF TYPICAL CONCENTRATOR SYSTEMS

As a means of exploring and illuminating the advantages and disadvantages of various levels of circuit redundancy, the fault tolerance of a cross-section of typical concentrator circuit designs has been computed using the above described methodology.

Table 1 provides values of the various parameters used in the study example to illustrate the methodology; these parameters are the number of parallel cell strings, number of cells per bypass diode, nominal array size, number of cells per source circuit, source-circuit voltage, and cell and module max-power voltage.

The bypass-diode frequencies used span the range from one diode across every cell to one every thirty cells. Since hot-spot protection

considerations suggest a maximum of 10 cells per diode, 30 cells per diode represent an upper bound only useful for a module design with excellent cell cooling and resistance to thermal deterioration. It is also representative of the maximum number of series cells typically mounted in a single module.

Table 1. Array/Module Circuit Parameters

Number of Parallel Cell Strings.....	1,4,8,16
Number of Cells/Bypass Diode.....	1,4,6,8,10,15,20,30
Nominal Array Field Peak Power.....	100 MW
Number of Cells/Source Circuit.....	1800
Source-Circuit Voltage.....	1000 Volts
Cell Max-Power Voltage.....	0.555 Volts
Module Max-Power Voltage.....	17 Volts

In lieu of field experience data, cell failure rates were selected based on what can be reasonably tolerated in an array so that overly large power losses do not occur over the lifetime of the array. Based on this, yearly cell failure rates of 0.001 and 0.0001 were used.

Before examining the parametric results it is useful to consider the detailed calculations of a representative example involving a single-string source circuit. This is an important circuit configuration for concentrator arrays for it allows the cells on a single array to be connected in series, simplifying wiring and resulting in lower currents. Assumed circuit parameters include:

System voltage.....	1000 volts
No. of series cells/source circuit.....	1800
No. of parallel cell strings/source circuit.....	1
No. of series cells/substring.....	10
No. of series blocks/bypass diode.....	1
No. of series blocks/source circuit.....	180

With the assumed 1000 volt system, the number of series cells per source circuit (1800) was obtained by dividing 1000 by an assumed 0.555 volts per solar cell. To achieve a reasonable endurance to hot-spot heating, a bypass diode was assumed around every 10 series cells; this gives 10 cells per substring. Because no paralleling is used, the size of the series block is established by the frequency of placement of the bypass diodes; the number of series blocks per source circuit (180) is thus 1800 cells divided by 10 cells per diode.

Next, the fraction of failed cells throughout the PV system life must be estimated. If we assume an annual failure rate of one per thousand cells and no replacement, the fraction of failed cells after the 5th, 10th, 15th, 20th, and 30th year will be 0.005, 0.010, 0.015, 0.020 and 0.030.

The next step is to compute the substring failure densities corresponding to these cell failure densities. Using Equation 1 we obtain respectively: 0.049, 0.096, 0.140, 0.183, and 0.263. The array power loss

fraction is finally determined for each of these cases from Figure 2 (or the array power loss fraction graph on page B-2 in Appendix B). Note that the set of curves in Figure 2 is for single-string source circuits with one series block per bypass diode. In the example case, interpolation is used to find a value of the array-power-loss fraction appropriate for 180 series blocks per source circuit. The array-power-loss fraction for each time period considered is: 0.06, 0.10, 0.20, 0.30, and 0.40 respectively, i.e., this array will be degraded by 40% at the end of 30 years with a cell failure rate of one per thousand per year.

Results for multiple parallel-string source circuits are obtained in exactly the same way by interpolating among the graphs in Appendix B for parallel configurations.

Examining Appendix B, one will also note that different graphs are provided for two different cell I-V curve fill factors of 0.70 and 0.76; fill factor is $P_{mp}/(I_{sc} \times V_{oc})$ and is a measure of how rectangular the I-V curve shape is. Note that the better (higher) the fill factor the more intolerant the array is to open circuits. This implies that very high efficiency arrays of the future may have to increase the level of circuit redundancy to achieve the same level of fault tolerance as present, less efficient (lower fill factor) arrays.

Figures 3 and 4 summarize the results for the cases considered by providing the array power loss fraction as a function of time. Note that optimal fault-tolerance considerations indicate that either single-string source circuits or multiple parallel strings, of the order of twelve or more in parallel, provide the best fault tolerance for cases that are of practical importance. Note that low numbers of parallel strings, such as 4 to 8, only provide improved fault tolerance with large numbers of cells per diode; these large numbers of cells per diode are inconsistent with the requirements of tolerance to hot-spot heating.

Modest numbers of parallel strings (such as 4 to 8) lead to greater losses because the remaining (n-1) parallel cells are incapable of carrying the over-current resulting from the open circuiting of one of the substrings. As a result, the cells go into reverse bias, the bypass diode conducts, and the entire series block is lost as a power generator. Only when there are a sufficient number of parallel cells to handle the over-current, does paralleling have an advantage from a fault tolerance point of view.

Figure 5 gives a plot of the time to reach a level of array power loss of ten percent as a function of source-circuit series-parallel configuration, assuming a yearly cell failure rate of one per thousand and no module replacement. The figure again confirms that the single-string source circuit has a distinct advantage over a moderate amount of paralleling of cell strings (4-8 parallel strings), but is at a slight disadvantage (for >4 cells per bypass diode) compared to a large degree of paralleling (16 parallel strings). However, the slight gain in fault

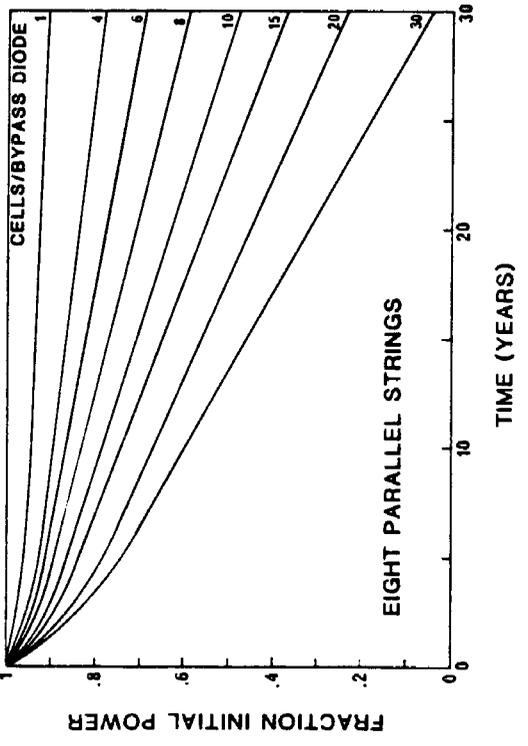
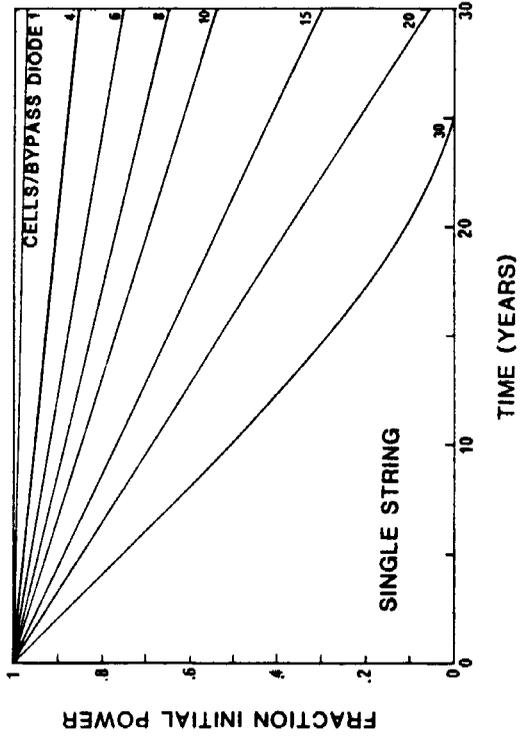
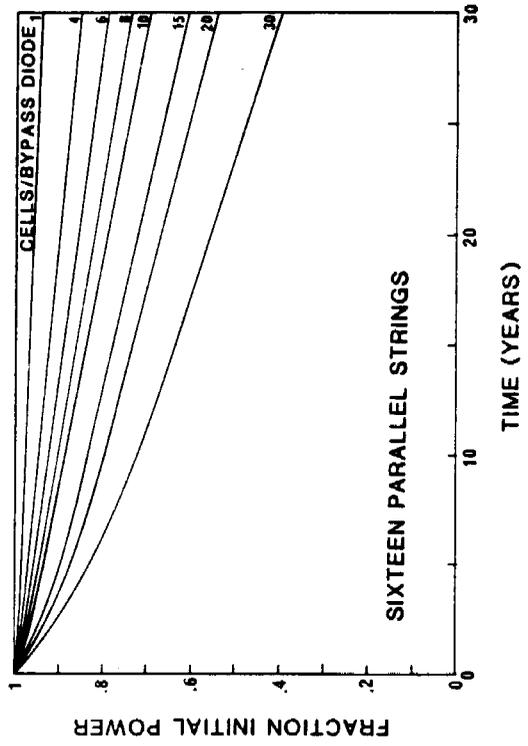
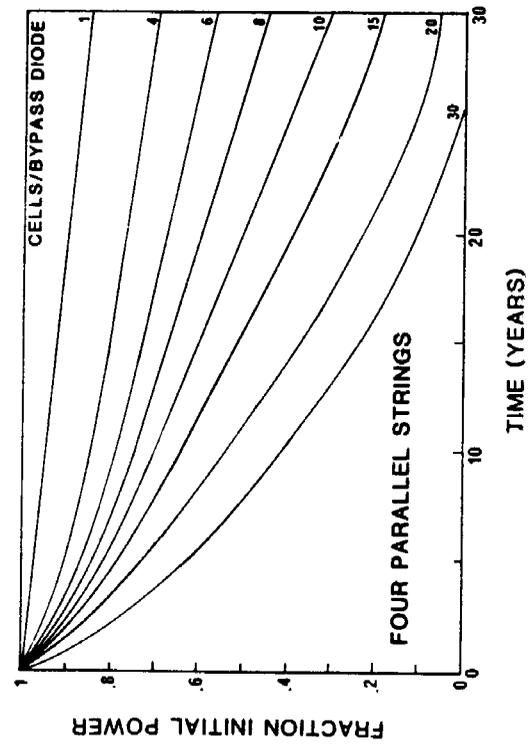


Figure 3. Array Power Loss vs Time for a 0.001 Cell Annual Failure Rate and Various Series-Parallel Configurations

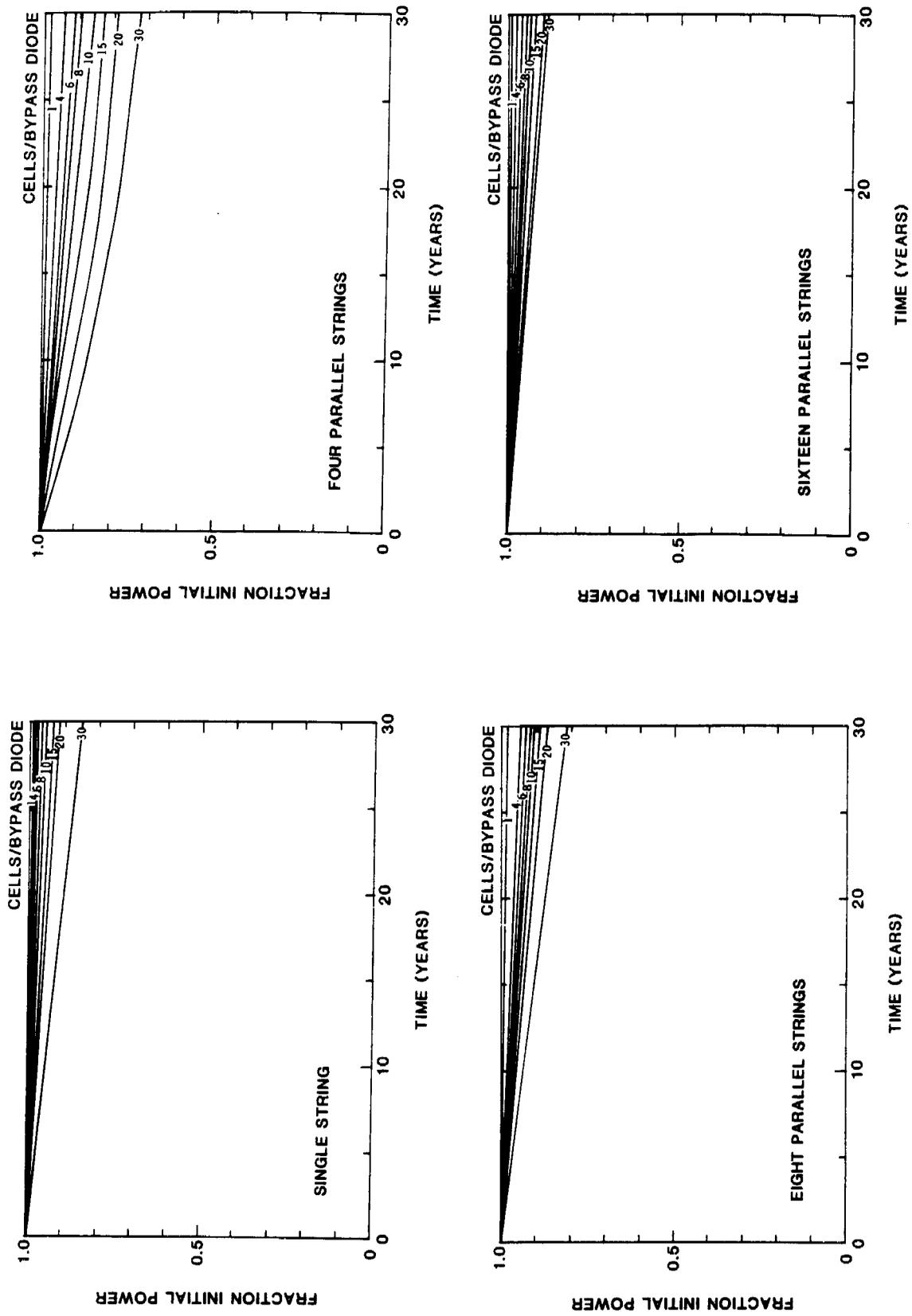


Figure 4. Array Power Loss vs. Time for a 0.0001 Cell Annual Failure Rate and Various Series-Parallel Configurations

tolerance to open-circuit cells also could be achieved by increasing the number of bypass diodes, which also provides added protection against hot-spot heating.

In the absence of economic trade-off considerations, discussed in the next section, the optimal array-circuit configurations, without module replacement, can be selected from Figures 3 and 4 for a given size system (voltage), yearly cell failure rate, and desired array lifetime. Of course, other considerations besides the array power loss fraction must be taken into account when appropriate.

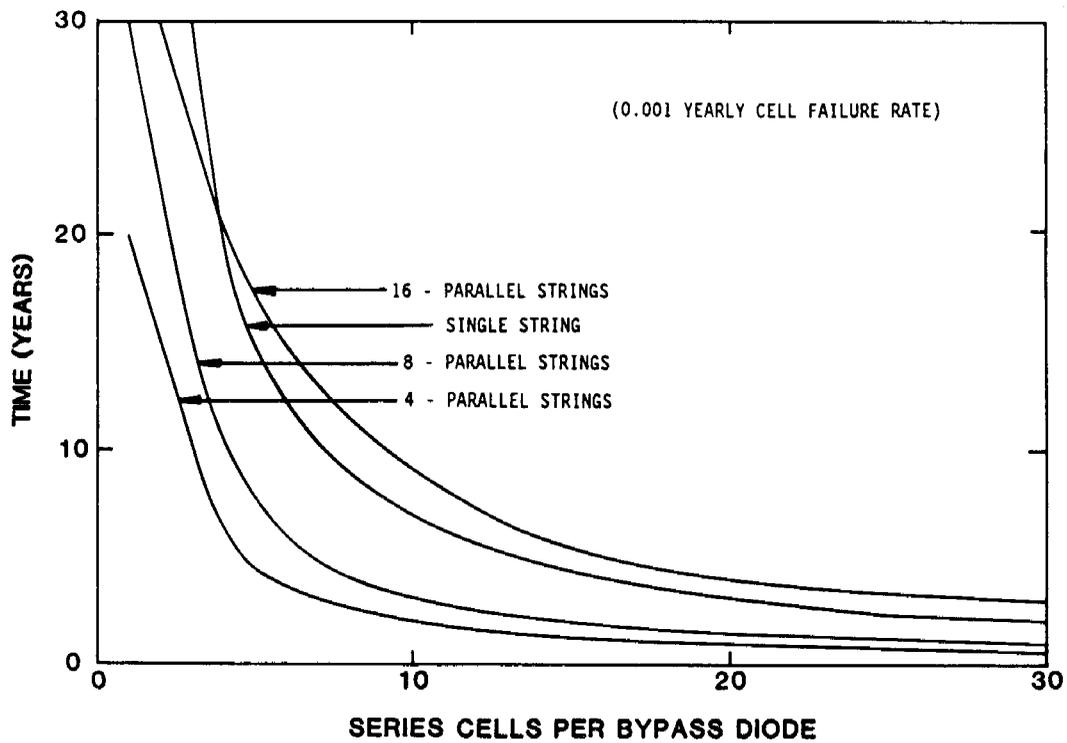


Figure 5. Time to Reach 10% Array Power Loss vs. Number of Cells/Bypass Diode

SECTION III

CIRCUIT LIFE-CYCLE COST OPTIMIZATION

A. COST OPTIMIZATION METHODOLOGY

Although single-series-string source circuits are shown above to have important fault tolerance advantages, they also require a maximum number of bypass diodes. To properly assess the true optimum concentrator array circuit strategy it is necessary to examine the total life-cycle energy costs associated with the various circuit configurations, including alternative maintenance and replacement strategies.

Module replacement adds an important dimension to the problem and brings economics into the picture when tradeoffs are made between the present value of the cost of module replacements and the present value of the energy lost by not replacing modules.

A useful approach to determining optimum replacement strategies for modules with failed cells is to determine the maximum ratio of life-cycle benefit to life-cycle cost through a parametric study where life-cycle benefit and life-cycle cost are defined by the following equations (Reference 4):

$$\text{Life-cycle benefit} = \sum_{i=1}^{30} RE_i(1+k)^{-i} \quad (2)$$

$$\text{Life-cycle cost} = C_0 + \sum_{i=1}^{30} C_i M_i (1+k)^{-i} \quad (3)$$

where:

- R = Cost (worth) of energy assumed constant over the plant lifetime in constant dollars (start-up-year \$/kWh)
- E_i = Energy generated in year i (kWh)
- C₀ = Initial plant cost (start-up-year \$)
- C_i = Cost per module replacement action (start-up-year \$/module)
- M_i = Number of modules replaced in year i
- k = Present value discount rate
- 30 = Plant lifetime (years) (assumed)
- i = index referring to year i

Maximizing the ratio of life-cycle benefits to life-cycle costs can be interpreted as, and is mathematically identical to, minimizing the break-even cost of delivered electricity:

$$R_{\text{break-even}} = \frac{C_0 + \sum_{i=1}^{30} C_i M_i (1+k)^{-i}}{\sum_{i=1}^{30} E_i (1+k)^{-i}} \quad (4)$$

Two numerical algorithms have been used at JPL to perform this optimization over the space of possible module replacement strategies. The first method uses a multivariate optimization program that repeatedly evaluates any arbitrary function of n variables and locates the values of the variables where the function is a minimum. For the problem at hand the function to be minimized is Equation 4, and the n variables are the 30 values of M_i representing the number of modules replaced in each of the thirty years of the photovoltaic system's life.

This algorithm has the advantage of being able to locate the least-cost replacement strategy independent of its complexity. However, it suffers the disadvantage of converging very slowly. An important finding from the use of this algorithm is that, in nearly all cases analyzed, the optimum replacement strategy has been either no module replacement at all, or module replacement each time a solar cell fails. In the rare cases in which one of these two options has not been optimum, the optimum replacement strategy has always been to fully replace failed modules in the first few years of the system's life, and then to replace no modules in subsequent years. For more details on the applicability of each strategy see Reference 4.

Based on this finding a second optimization algorithm has been developed based on selecting the least cost of 31 trial replacement strategies. The 31 trial strategies include no replacement at all, and module replacement for each cell that fails during the first through the N^{th} year ($N = 1, 30$) with no replacement for the balance of the plant's life. This algorithm works very efficiently and is the one used in this study.

B. COST OPTIMIZATION EXAMPLES

To illustrate the life-cycle-cost optimization procedure and explore the economic viability of the previously analyzed levels of circuit redundancy, two sets of economic parameters were used in example calculations that follow. The two sets of economic parameters will be referred to as the 15%-module-efficiency and the 20%-module-efficiency models. They are also referred to as the near-term and long-term models, respectively, because the parameters in the two models are meant to represent near-term and long-term module and array cost goals. The values of the parameters defined by these models, and which are inputs to Equations 2, 3, and 4, are given in Table 2. The values for the 15%-module-efficiency

model were obtained from Reference 5 and those for the 20%-module-efficiency model from Reference 6. The parameters associated with the near-term model represent module costs of \$1.85/W based on a 15%-efficient module and a yearly production of 70,000 modules (Reference 5). When energies are calculated for use in Equation 4 it is assumed that the 15% and 20% module efficiencies are reduced by a factor of 20% each to account for such factors as actual module efficiency at nominal operating temperatures, electrical wiring losses, soiling losses, tracking losses, etc.

Assumption of an efficiency value also determines values for non-economic parameters such as the number of modules replaced (e.g., an array field composed of lower-efficiency modules contains more modules and therefore more modules to replace); these values are also given in Table 2. The cost per module replacement action is the total cost (parts and labor) incurred as a result of the replacement action.

Values of additional economic parameters taken from Reference 7 are also given in Table 2. The array-field costs incorporate all array-associated costs including module costs, support structure and tracking, and intra-array-field wiring. The balance-of-system costs include site preparation and development, and power conditioning and associated wiring. A bypass-diode nominal cost of \$7.50 per diode (30-A capacity), including heat sink and installation, was assumed based on actual experience with similar diodes in multi-megawatt flat-plate central station applications.

The annual array energy production was determined using a value of 1880 kWh/m² per year for direct normal annual irradiance, which is typical of a site such as Albuquerque, NM.

Table 2. Economic Parameters Used in Life-Cycle Benefit/Cost Analyses

Array-Field Cost	
15% Model (\$322/m ²).....	\$2.69x10 ⁸
20% Model (\$277/m ²).....	\$1.73x10 ⁸
Balance-of-System Cost	
15% Model.....	\$1.65x10 ⁷
20% Model.....	\$1.60x10 ⁷
Cost per Module Replacement	
15% Model (3.67m ² Module Area).....	\$875
20% Model (2.75m ² Module Area).....	\$350
Number of Modules Replaced/Year	
Yearly Cell-Failure Rate=0.001	
15% Model.....	6820
20% Model.....	5460
Yearly Cell-Failure Rate=0.0001	
15% Model.....	704
20% Model.....	563
Discount Rate.....	0.09/Year
Inflation Rate.....	0.05/Year

Since single string source circuits were shown above to have important fault tolerance attributes, they were chosen for the example analysis. However, the principles that are illustrated apply to multiple-parallel-string source circuits as well. The only circuit-configuration parameter varied in the analyses was the number of cells per bypass diode.

As discussed above, the replacement strategy assumes module replacement options involving no replacement at all, and replacement through the first N years out of thirty, followed by no replacement after year N. The optimum value of N is that which leads to the lowest break-even cost of electricity; it varied between 0 and 30 for the given set of input parameters.

Figure 6 provides typical results obtained for the optimum level of module replacement as a function of the number of cells per bypass diode for the two module efficiencies and two yearly cell-failure rates. The figure shows that the optimum number of years of module replacement increases with the number of cells per bypass diode; this is because of the greater amount of energy lost with widely spaced diodes. Note that for practical systems with less than 10 cells per diode, no module replacement is the optimal strategy. The level of replacement is slightly greater for the 20%-module-efficiency model, because module-replacement cost is less, and, therefore, a greater amount of module replacement is more cost effective than for the 15% model.

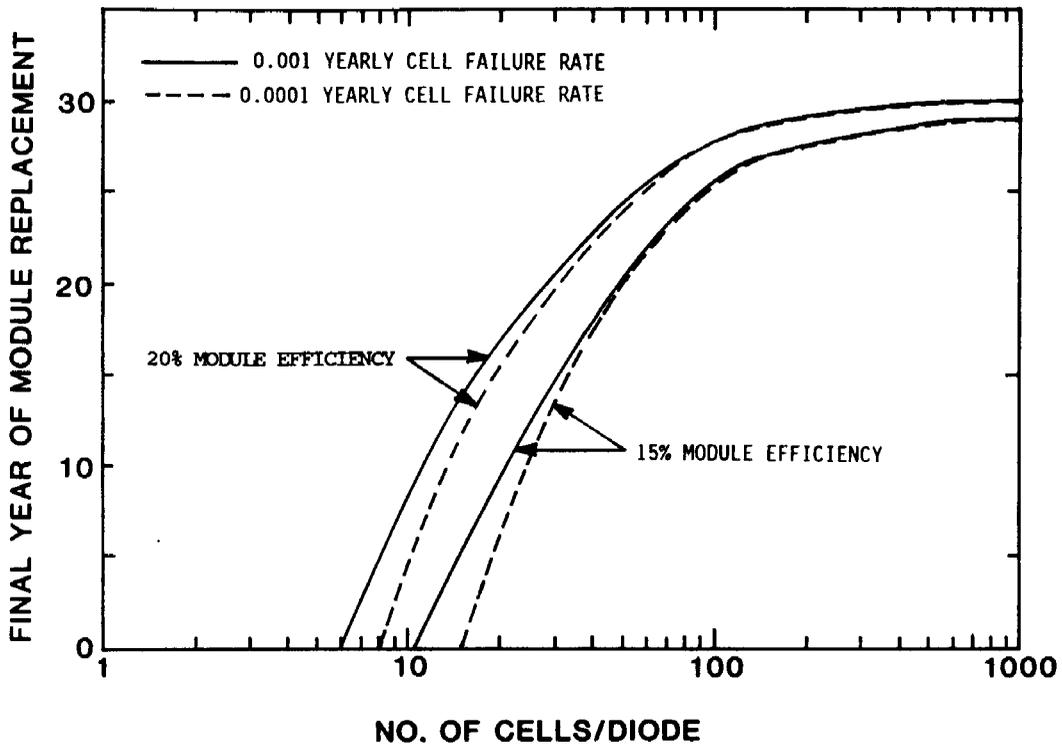


Figure 6. Optimal Module Replacement Strategy in Terms of Final Year of Replacement vs. Number of Cells/Bypass Diode

The sensitivity of the value of the economic parameters in Equations 2 and 3 to the bypass diode frequency can be determined by obtaining the break-even value of the parameter in question, keeping all other parameters constant except the number of bypass diodes. The break-even value is that value that leads to a life-cycle benefit/cost ratio of one.

Figure 7 gives separate plots of the break-even values of the energy worth, everything else held constant, as a function of the number of cells per bypass diode for the 20%-efficient module, and yearly-cell-failure rates of 0, 0.0001, and 0.001. The zero-failure-rate case represents the system cost, including bypass diodes, without energy lost and cost of module replacement. In all of the plots, the values of energy worth are normalized to the values for the zero-failure mode and the case of one bypass diode per cell. These values are \$0.114/kWh and \$0.168/kWh respectively for the 20% and 15% efficient modules.

Figure 7 shows a striking contrast between the two failure rates considered. The 0.001-failure-rate case has the minimum break-even cost at four cells per diode, while the break-even cost for the 0.0001-cell-failure-rate case decreases monotonically as the number of cells per diode increases. Since significant hot-spot heating is expected in most concentrator modules with more than 10 cells per bypass diode, it is both prudent and economically reasonable to incorporate a modest number of bypass diodes (at least every 10 to 20 cells depending on the module's hot-spot endurance) into the circuit design. For higher failure rates the optimum frequency is seen to increase to the 4 per diode noted for a failure rate of 0.001.

Figure 8 provides the same plot for a 0.001 failure rate with a breakout of the contributions of the two cost components, one for lost energy, and the second for module replacement. Note that energy is lost only during those years when no module replacement occurs; i.e., it is assumed that if modules are replaced, they are replaced quickly so that no energy is lost. Figure 8 shows that the optimum bypass-diode-placement strategy (minimum break-even cost) occurs at four cells per diode; this is in the region on the curve where no module replacement is the optimum replacement strategy.

Figure 9 provides plots of the same parameters for the 0.0001-cell-failure-rate case that Figure 8 provided for the 0.001 case. Although the break-even cost decreases monotonically with increasing number of cells per diode, the region where no module replacement is optimum occurs at about the same number of cells per diode as the 0.001-cell-failure-rate case.

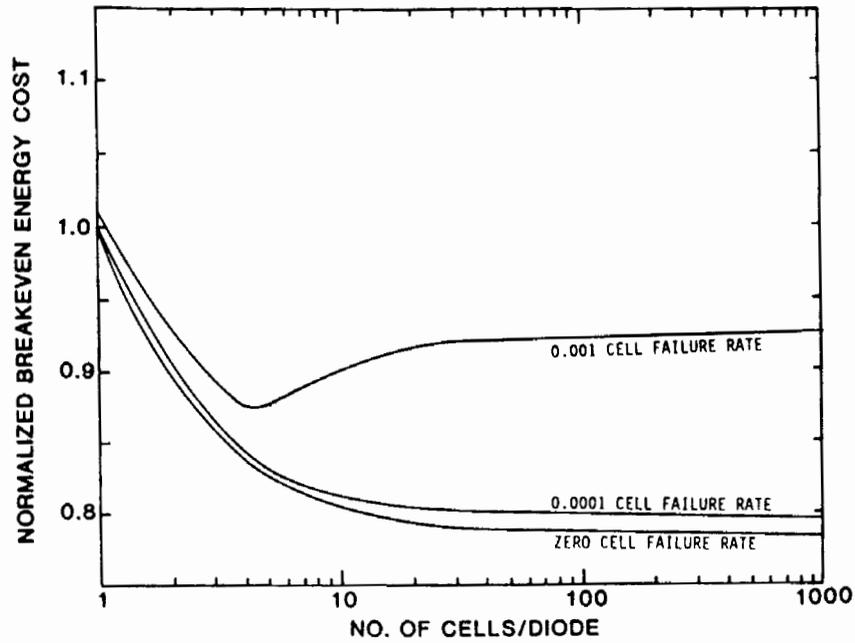


Figure 7. Break-Even Values of Energy Worth vs. No. of Cells/Bypass Diode for Single-String Source Circuit, 20% Efficiency

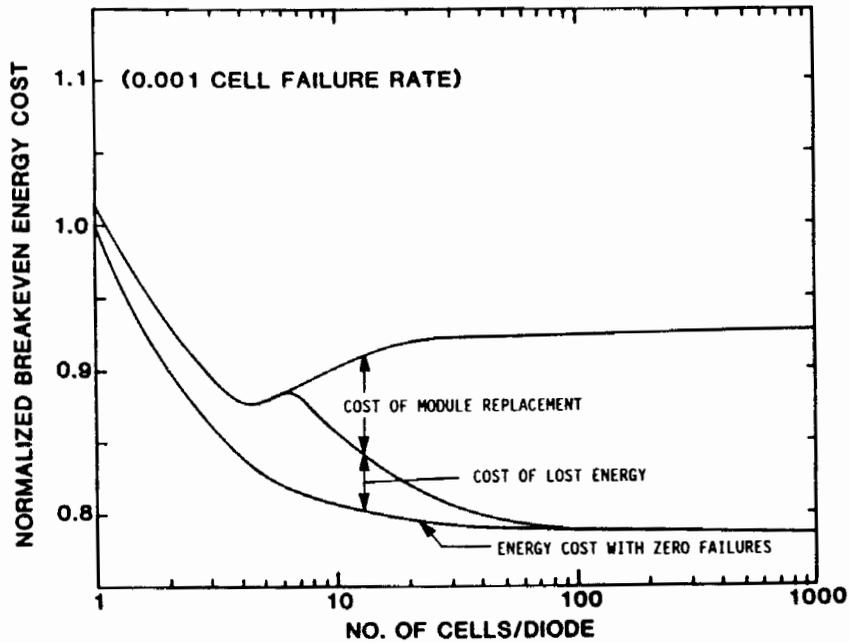


Figure 8. Cost Separation of Break-Even Values of Energy Worth vs. No. of Cells/Bypass Diode for Single-String Source Circuit, 20% Efficiency and 0.001 Cell Annual Failure Rate

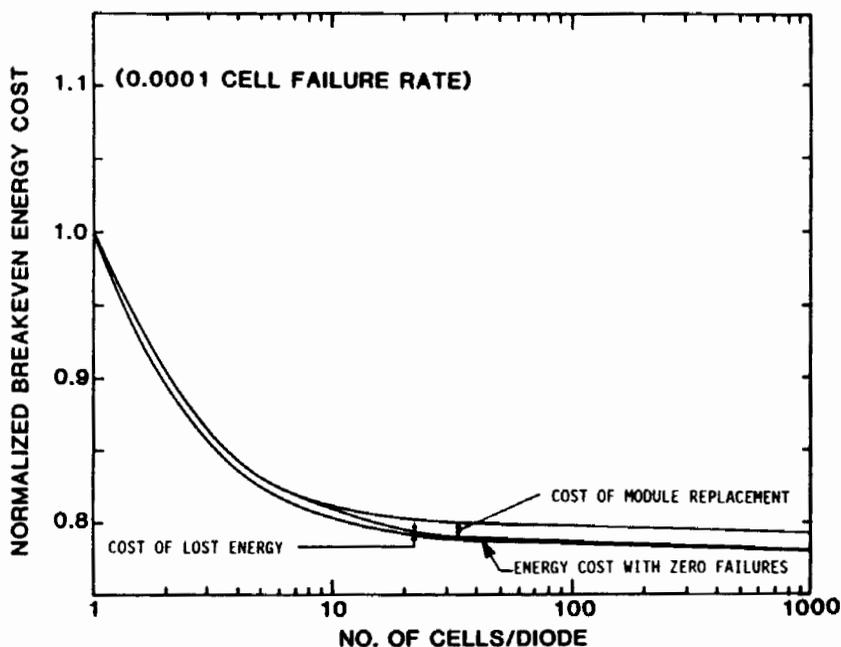


Figure 9. Cost Separation of Break-Even Values of Energy Worth vs. No. of Cells/Bypass Diode for Single-String Source Circuit, 20% Efficiency and 0.0001 Cell Annual Failure Rate

Figure 10 provides break-even values of energy worth for the same failure rates for the 15%-efficiency model that Figure 7 provided for the 20% model. Again the 0.001-failure-rate case shows an optimum cost at a diode frequency of one diode every four cells, and the 0.0001 case shows a monotonically decreasing cost with fewer diodes. The latter begins to level off to its asymptotic value at a higher diode frequency (one every ten cells) than was the case for the 20%-efficiency model. In summary, the results provided by the two failure rates argue for diodes every 4 to 10 cells.

Figures 11 and 12 provide plots for the 15%-efficiency model, comparable to those that Figures 8 and 9 provide for the 20% case; the conclusions drawn from Figures 8 and 9 mirror those discussed above for the 20% case.

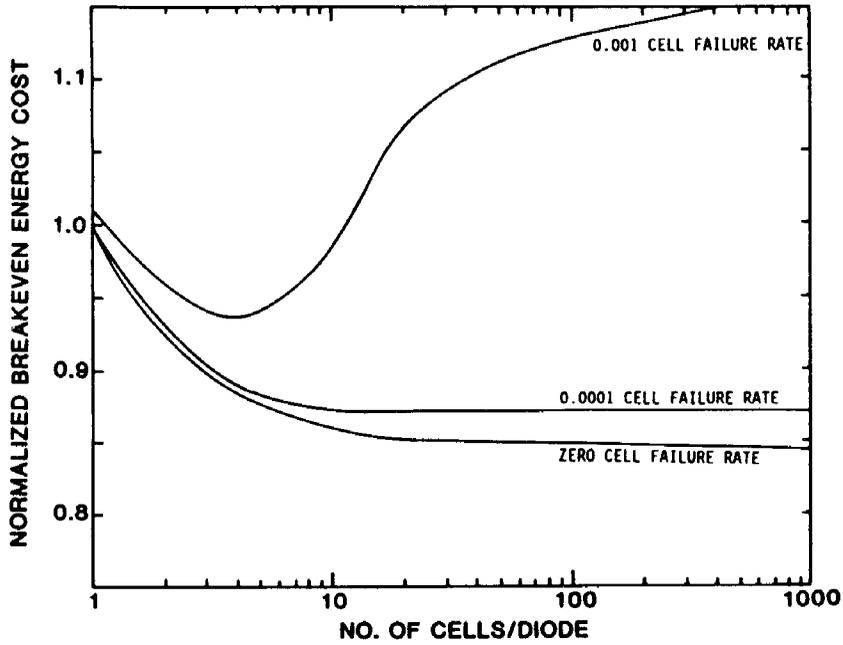


Figure 10. Break-Even Values of Energy Worth vs. No. of Cells/Bypass Diode for Single-String Source Circuit, 15% Efficiency

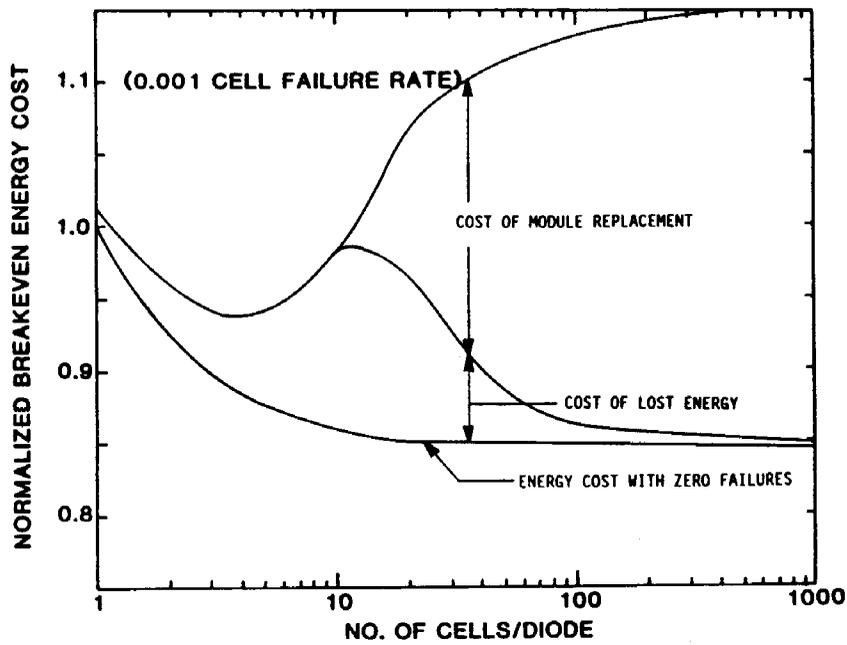


Figure 11. Cost Separation of Break-Even Values of Energy Worth vs. No. of Cells/Bypass Diode for Single-String Source Circuit, 15% Efficiency and 0.001 Cell Annual Failure Rate

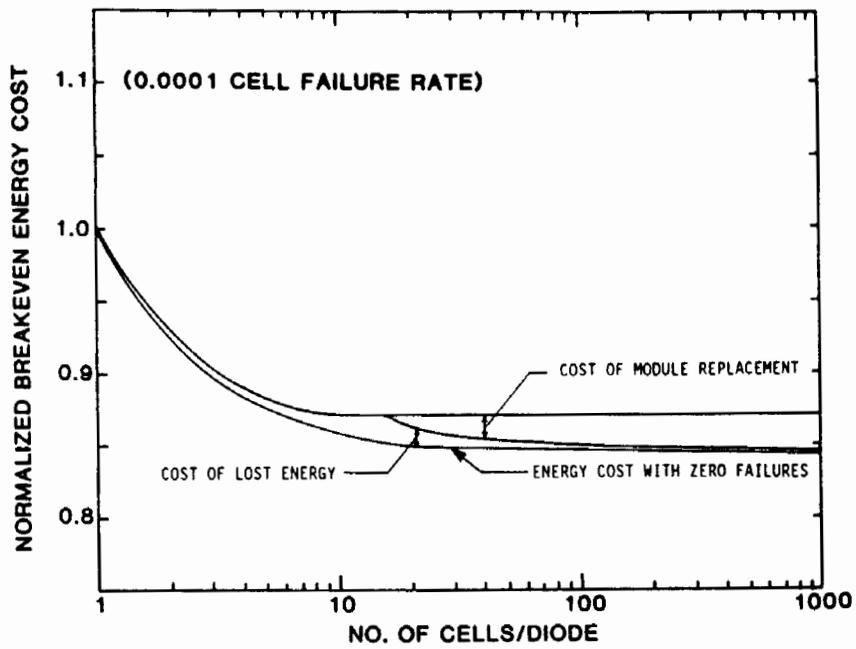


Figure 12. Cost Separation of Break-Even Values of Energy Worth vs. No. of Cells/Bypass Diode for Single-String Source Circuit, 15% Efficiency and 0.0001 Cell Annual Failure Rate

SECTION IV

RECOMMENDATIONS AND CONCLUSIONS

A. RECOMMENDED ARRAY CIRCUIT CONFIGURATION AND BYPASS DIODE FREQUENCY

The results of the analyses indicate that the optimal array series-parallel configuration is either single-string source circuits or multiple-string source circuits with large numbers of parallel strings (12-or-greater parallel strings). The choice between these two strategies will largely depend on the economies of the components, such as bypass diodes, cabling and connectors, required to carry the source-circuit current. Previous experience with large flat-plate arrays suggests that current levels on the order of 50 to 150 A are quite cost effective in large central-station systems. If this same range holds true for concentrator modules, multi-parallel-cell source circuits will be advantageous for large systems using concentrator modules with individual cell currents less than around 10 A. One of the reasons for the efficiency of this circuit design is that it allows the cost effective use of one large bypass diode for a module or group of parallel modules. For high-current cells (20 A or more), or low-power systems, single-string circuits may be the best choice.

Based on the economies of large bypass diodes, the analysis suggests (Figure 7) that it is not cost effective to use the diodes more frequently than one for every 4 series cells. Similarly there is little advantage to be gained with fewer than one diode for every 10 to 20 series cells. Because hot-spot protection argues for one diode every 10 series cells or less, the optimum frequency appears to be in the range of 4 to 10 series cells per diode, depending on the actual cost per diode and the expected cell-failure rate.

B. RECOMMENDED MODULE REPLACEMENT STRATEGIES

Analyses were also conducted to determine the optimum module replacement strategy based on minimizing the total break-even cost of photovoltaic energy produced. In general, when a circuit design with optimal fault tolerance is used, the optimum replacement strategy is no replacement. Only when less fault tolerance is introduced, or where significantly less expensive modules are used, does a strategy of replacement become desirable.

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APPENDIX A

METHODOLOGY FOR DETERMINING ARRAY POWER LOSS

Certain faults occur in terrestrial photovoltaic modules, both at the beginning of life and throughout the duration of field operation. Computing the array-field power degradation corresponding to various levels of random open-circuit cell failures is critical to understanding both the quantitative significance of various cell failure levels, and the benefits of candidate fault-tolerance circuit-design strategies. The problem is made particularly difficult by the non-linear electrical behavior of solar cell networks (particularly with bypass diodes) and by the presence of millions of cells and diodes in a typical megawatt-scale PV power plant. This appendix describes the method developed and presents sample results of the extensive parametric analyses performed leading to the set of computation-assisting graphs provided in Appendix B.

The nomenclature used in this appendix is described in Section I of this report, in connection with Figure 1, and will not be discussed further here.

A. ANALYTICAL APPROACH

The developed approach incorporates a combination of statistical analyses to determine the probability of various cell-failure physical distributions, together with precision I-V curve power-degradation computations to quantify resulting power losses. The computer-assisted method is most easily viewed as containing the following five steps:

- (1) Computation of the fraction (F_{SS}) of failed substrings in the array field corresponding to the given fraction (F_C) of open-circuit cell failures.
- (2) Computation of the fraction of series blocks that contain specific numbers of failed substrings; this is done for various substring failure fractions.
- (3) Calculation of the fraction of source circuits containing different levels of degraded series blocks.
- (4) Calculation of power-loss fractions for source circuits containing the computed distributions of series blocks with specific numbers of failed substrings.
- (5) Determination of the weighted sum of the degraded source-circuit power-loss fractions; this value is the total power-loss fraction of the array field.

The details of these steps are described below.

1. Determination of the Fraction (F_{SS}) of Open-circuit Substrings

The substring (see Figure 1 in the body of the report) is the fundamental building block of the array field; it is the element that is wired in parallel to create a series block. The fraction of open-circuit substrings is mathematically tied to the fraction of open-circuit solar cells by the binomial distribution equation:

$$f(x) = n!/(x!(n-x!))(P^xQ^{n-x}) \quad (A-1)$$

where $f(x)$ is the probability of the occurrence of x events in n trials, if the probability of occurrence of the event in any given trial is P , and $Q = 1-P$ is the probability of the event not occurring.

For the case at hand the fraction of open circuit substrings is equal to the probability of any given substring containing one or more failed solar cells, or one minus the probability of any given substring containing no failed solar cells. Substituting into Equation A-1 with $x = 0$, $n =$ number of cells per substring, and $P =$ probability of any given solar cell being open-circuit gives:

$$F_{SS} = 1 - (1 - F_C)^{N_C} \quad (A-2)$$

where:

F_{SS} = substring failure density

F_C = cell failure density

N_C = number of cells per substring

Equation A-2 is exact providing that the solar cell failures are statistically independent occurrences, i.e., the failure of one cell does not influence the failure of another.

2. Computation of the Fraction of Series Blocks with Specific Numbers of Failed Substrings

With the fraction (or density) of failed substrings determined, the next step is to compute the fraction (probability) of series blocks containing a specific number (x) of failed substrings. This is again defined by the binomial distribution (Equation A-1), this time with $n =$ the number of parallel substrings, and $P = F_{SS}$. The result of the analysis is a plot, such as Figure A-1 for each candidate number of parallel cell strings. Notice that Figure A-1 gives the fractions for all possible numbers of failed substrings as a function of substring failure density. Similar plots were also generated for 4 and 16 parallel substrings.

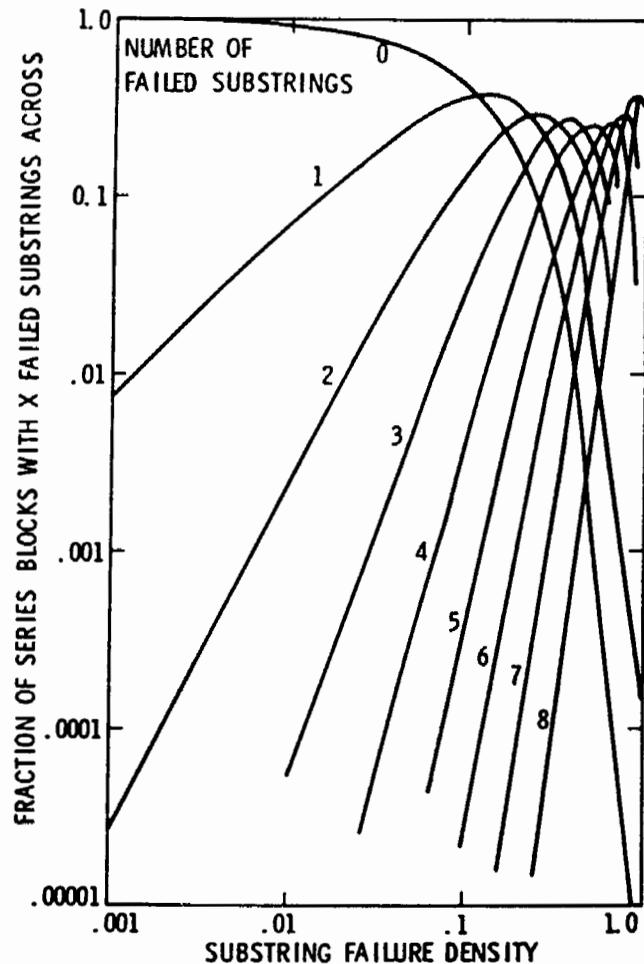


Figure A-1. Fraction of Series Blocks with a Given Number of Failed Substrings as a Function of Substring Failure Density, Eight Parallel Strings

3. Calculation of Source Circuit Degradation Distribution

Given the fraction of series blocks with various numbers of failed substrings, the next step is to determine the fractions of source circuits with various levels of these degraded series blocks.

A key measure of the level of source-circuit degradation is the extent to which a given source circuit contains series blocks with large numbers of failed substrings. This determination is broken into two separate statistical computations, based on the binomial equation (Equation A-1), but significantly more complex than those discussed at the substring and series-block level.

The first determination is the fraction of all source circuits whose worst-case series blocks have a particular number (x) of failed substrings. For example, with a four-parallel-string source circuit, some source

circuits may contain no failures at all, some may contain degraded series blocks containing a maximum of one failed substring, and others may contain degraded series blocks with a maximum of two, three, or four failed substrings, respectively. The results of this analysis are displayed in Figure A-2 as a function of substring failure density (F_{SS}). Similar graphs were generated for the cases of 8 and 16 substrings in parallel.

The second statistical determination is the fraction of series blocks in each source circuit that contain the same number of failed substrings as the worst-case series block. This analysis leads to results similar to those depicted in Figure A-1, except that the results specifically address the actual integer number of series blocks in a source circuit.

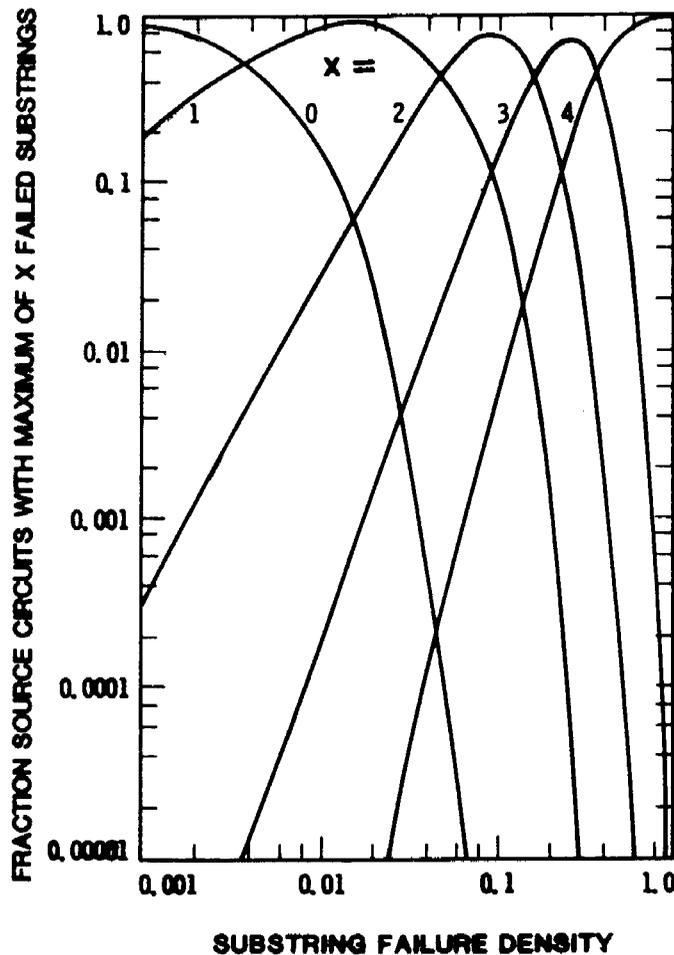


Figure A-2. Fraction of 4-Parallel-String Source Circuits With a Given Maximum Number of Failed Substrings

4. Calculation of Source-circuit Power Loss

With the fraction of source-circuits with various levels of failures computed, the final step is to determine the actual electrical power loss caused by the circuit element open-circuits. This step requires that the non-linear circuit behavior of the cell networks (and bypass diodes) be explicitly addressed.

This was done by constructing representative current-voltage (I-V) curves for each type of degraded series block (with diodes if applicable), and then numerically adding the I-V curves in series to obtain the resultant I-V curve for each type of degraded source circuit. The power degradation was obtained by subtracting the maximum power of the degraded source circuit from that of an undegraded source circuit.

The curve-addition and maximum-power-determination process demands a high level of precision and was entirely computer executed. To provide uniformity in the results, and to allow various cell fill factors to be dealt with explicitly, the series-block I-V curves were defined by the following empirical equation:

$$I = I_{SC} (1 - e^{(1.74/(0.87 - FF))(V/V_{OC} - 1)}) - V/R_{Sh} \quad (A-3)$$

where:

I = current at voltage V

I_{SC} = short-circuit current

FF = fill factor

V_{OC} = open-circuit voltage

R_{Sh} = shunt resistance

Degraded series blocks were modeled by appropriately scaling I_{SC} and R_{Sh} to reflect the loss of various numbers of parallel strings.

Because of the large number of cases involved, plots such as shown in Figure A-3, were generated for special-case source circuits where all degraded series blocks contain the same number of failed substrings. These were then used to interpolate the power loss for source circuits also containing degraded series blocks with fewer numbers of failed substrings.

Consider a source circuit having a fraction F_m series blocks with x failed substrings and F_{m-1} with x-1 failed substrings. If $F_m \sim F_{m-1}$, the series blocks with x failed substrings dominate and power loss can be computed based on them. However, if $F_m \ll F_{m-1}$, one of two possible cases arises. The first is the case in which the F_m series blocks dominate (similar to the case when $F_m \sim F_{m-1}$). The more difficult case to analyze occurs when the power loss due to the F_m series blocks is less than or equivalent to that with F_{m-1} series blocks.

To illustrate this latter case, consider the example of a source circuit having 2000 series blocks with $x = 2$, $x-1 = 1$, $F_m = .005$ and $F_{m-1} = .065$. This source circuit would have 10 series blocks with 2 failed substrings and 130 with 1 failed substring. A first source-circuit power loss would be determined from Figure A-3 for "Fraction of Failed Series Blocks" equal to 0.005 and the "Number of Failed Substrings" equal to 2. A second power loss would then be determined from Figure A-3 based on "Fraction of Failed Series Blocks" equal to 0.065 and "Number of Failed Substrings" equal to 1. The final power loss for the source circuit was estimated based on the results of the two separate determinations.

5. Determination of the Array Power Loss Fraction

Once the power loss of the various classes of degraded source circuits is available, the array power loss can be computed easily as the weighted sum of these losses, where the weights are the fractions of source circuits with a maximum of x failed substrings, for all values of x from 0 to the number of parallel strings in the source circuit. These fractions are displayed in Figure A-2 for the case of 4 parallel strings per source circuit.

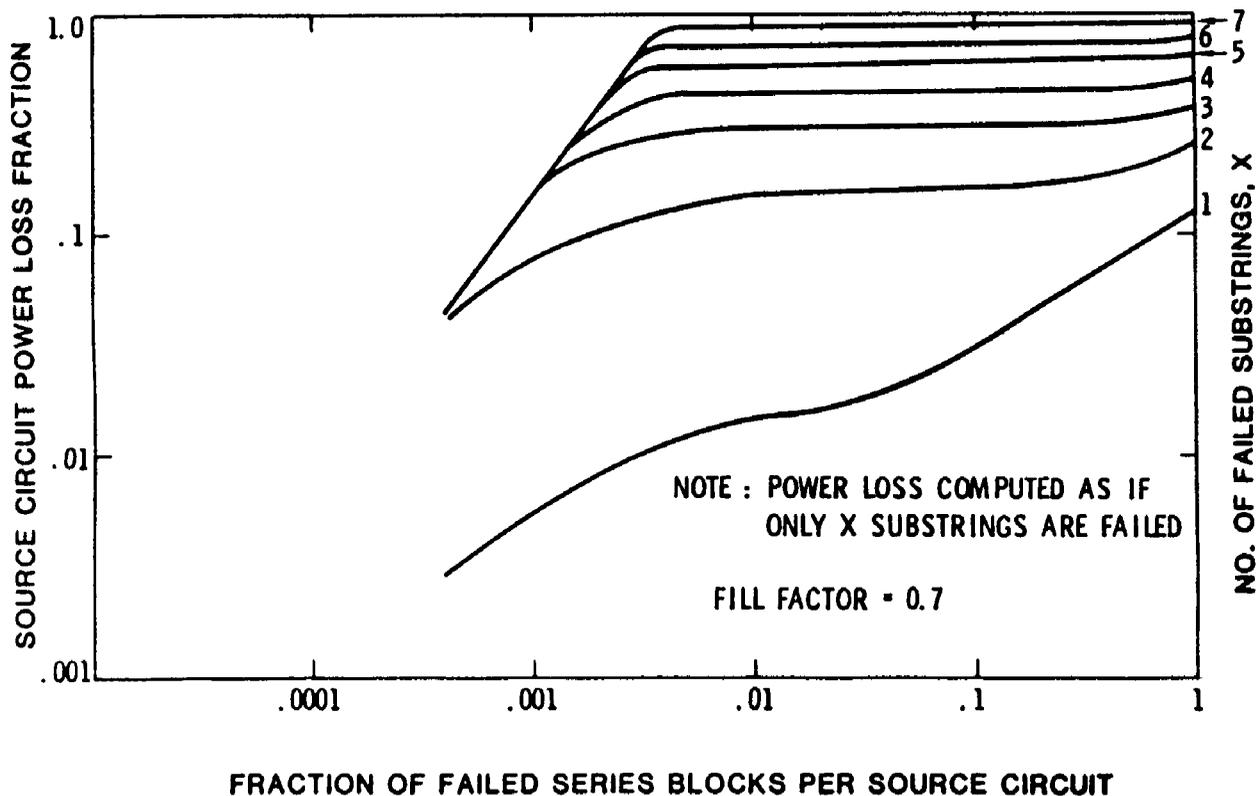


Figure A-3. Source-Circuit Power Loss as a Function of Failed Series Blocks for Eight Parallel Strings, Without Diodes

B. ARRAY POWER-LOSS FRACTION CURVES

Because of the complexity of the above method for determining the array power-loss fractions, steps 2 through 5 were repeatedly executed for a broad range of array parameter values so as to prepare a number of graphical curves that could be used for most system designs of interest. Figures A-4 and A-5 represent two example curves for the case of 8 parallel strings per source circuit, a cell fill factor of 0.70, and with and without bypass diodes. Appendix B contains a complete set of 24 graphs covering the following parameter ranges:

- o 1, 4, 8 and 16 parallel strings per source circuit
- o 1, 4, 8 and 12 series blocks per bypass diode
- o 0.70 and 0.76 fill factor

C. CONSTRAINTS AND CAVEATS

The analysis method described above, and the resulting curves in Appendix B, are directly applicable to a broad variety of PV-array designs. The use of the closed-form statistical treatment explicitly predicts the distribution of various levels of spatially-adjacent failures that is so important in the study of circuit redundancy. However, one limitation of the analysis is the assumption in some cases that the fraction of elements containing failures is the same as the probability that the element will contain a failure. This is only strictly true when the number of elements approaches infinity. In other words, the sample population being investigated must be large enough to be properly characterized by the probability distribution being used. For PV systems containing hundreds of source circuits, each with hundreds of series blocks, the approximation should be excellent. However, the approximations begin to deteriorate quickly when the number of elements drops to the level of 10 or less. The result of the poor approximation will be that small PV system may degrade significantly more or less than the predictable average system depending on the luck of the draw. This is analogous to trying to predict the output of 10 flips of a coin, as compared to an infinite number of flips, where heads and tails can each be expected to occur 50% of the time.

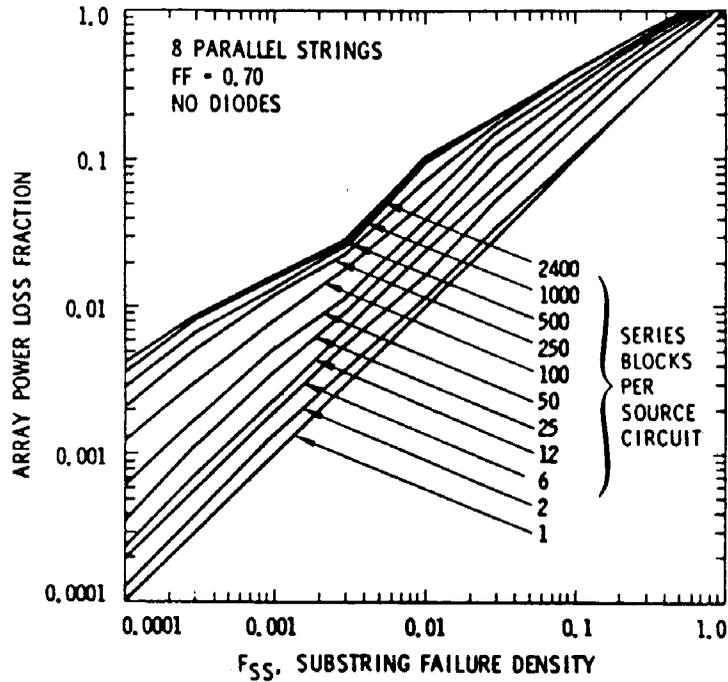


Figure A-4. Array Power Loss as a Function of Substring Failure Density for Eight Parallel Strings, Without Diodes

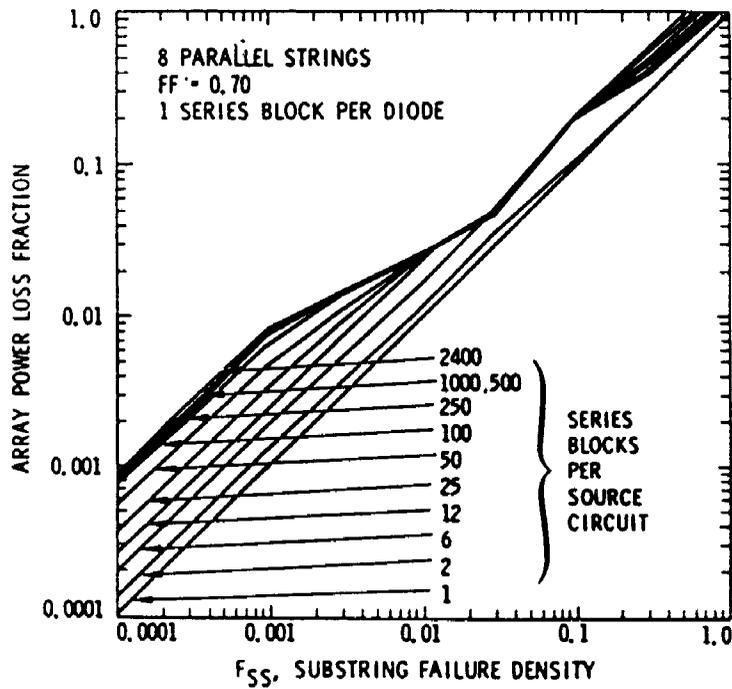


Figure A-5. Array Power Loss as a Function of Substring Failure Density for Eight Parallel Strings, With One Diode per Series Block

APPENDIX B

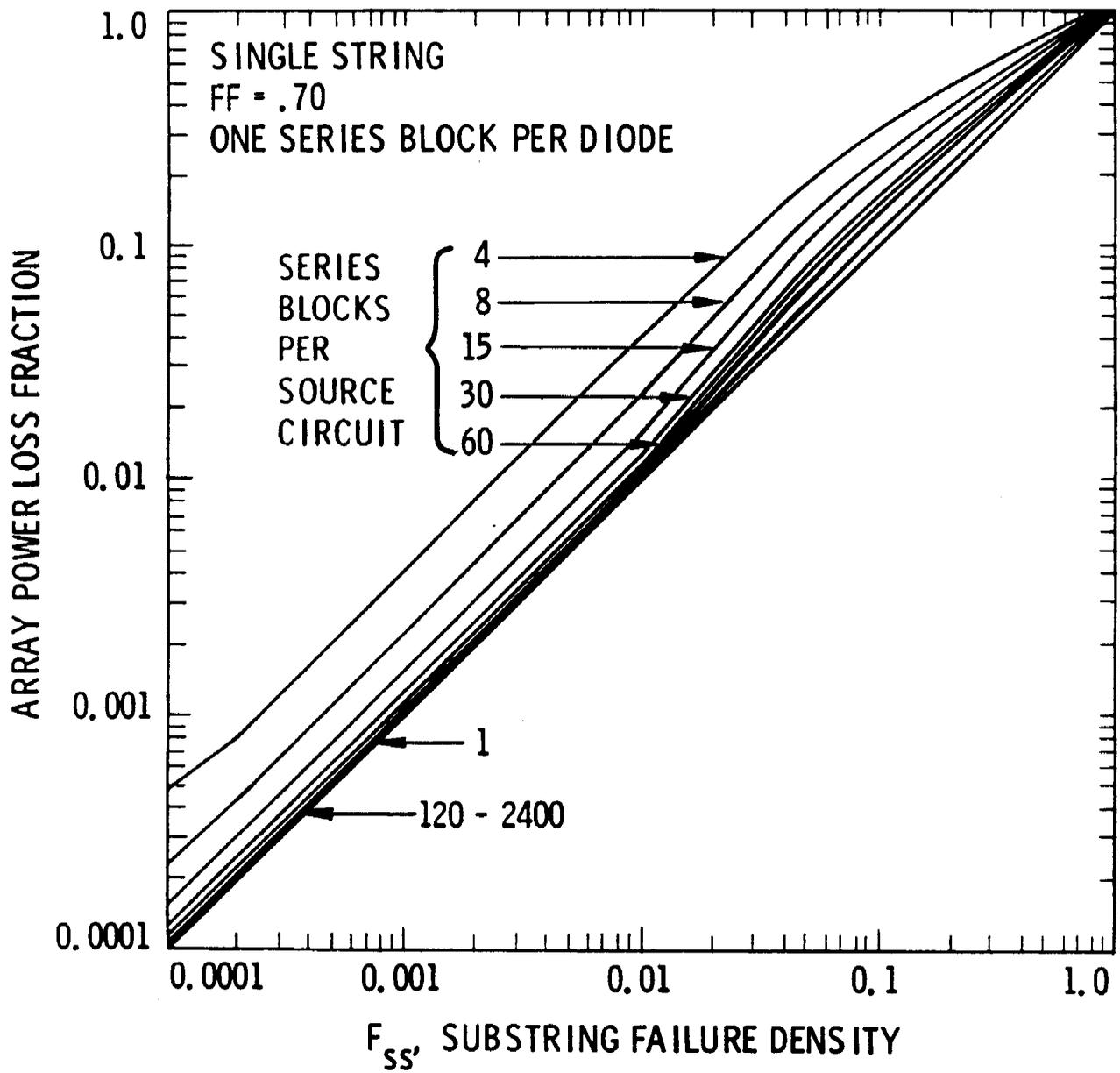
ARRAY POWER LOSS FRACTION CURVES

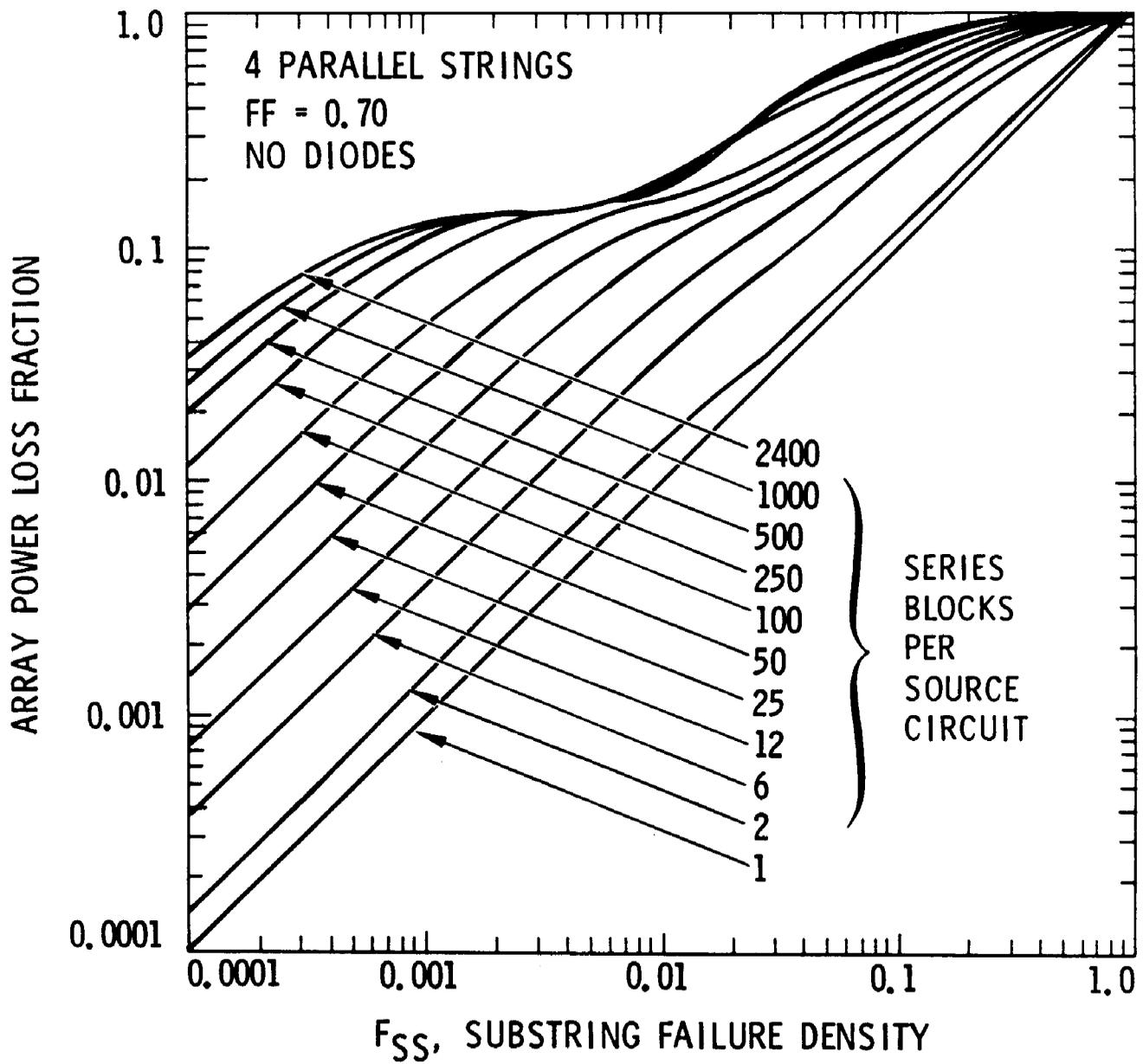
This appendix provides a collection of array-power-loss-fraction curves; a separate graph is included for each combination of the following parameters:

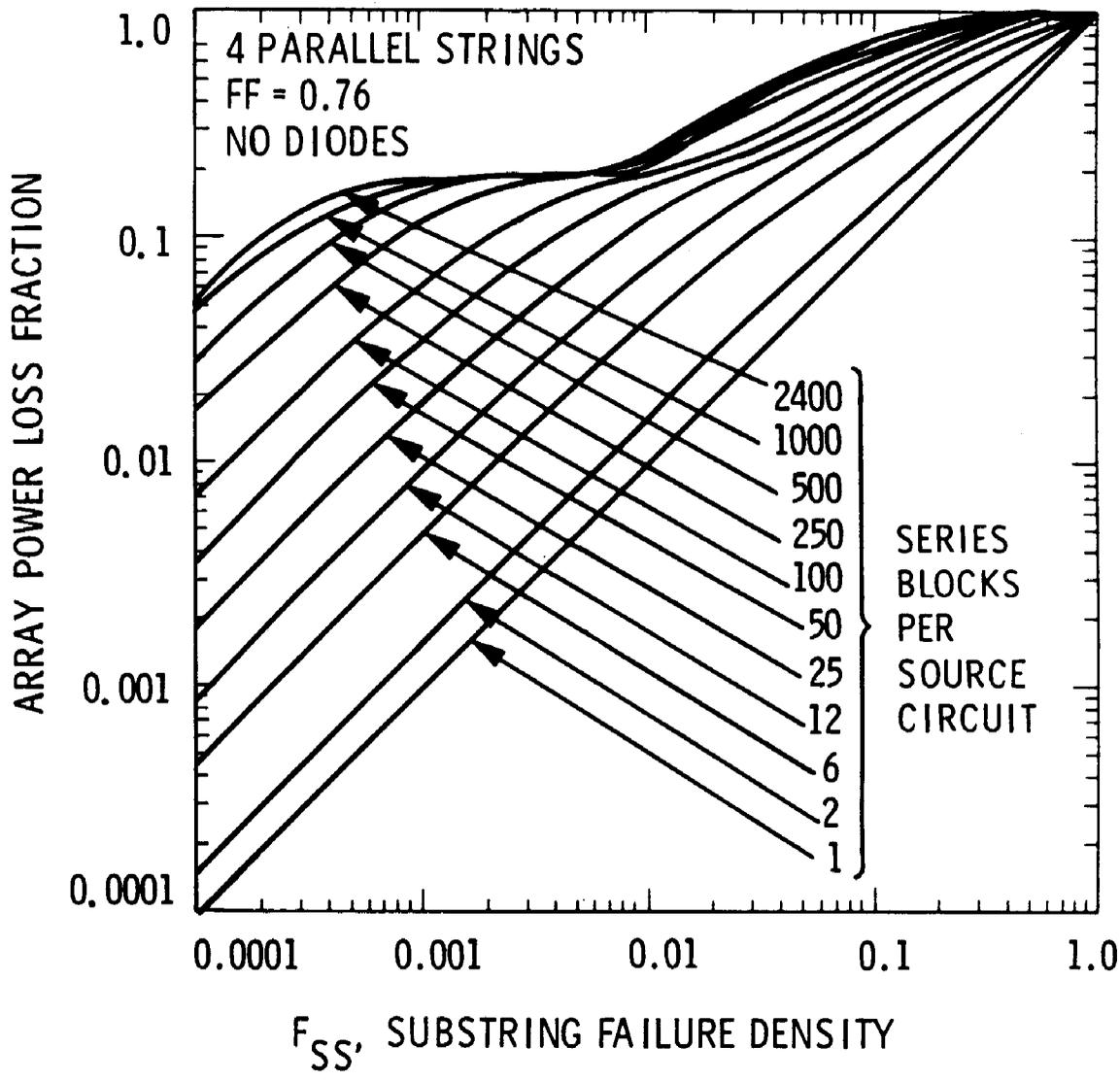
- (1) The number of parallel cell strings per source circuit
- (2) The cell fill factor (FF)
- (3) The number of series blocks per bypass diode

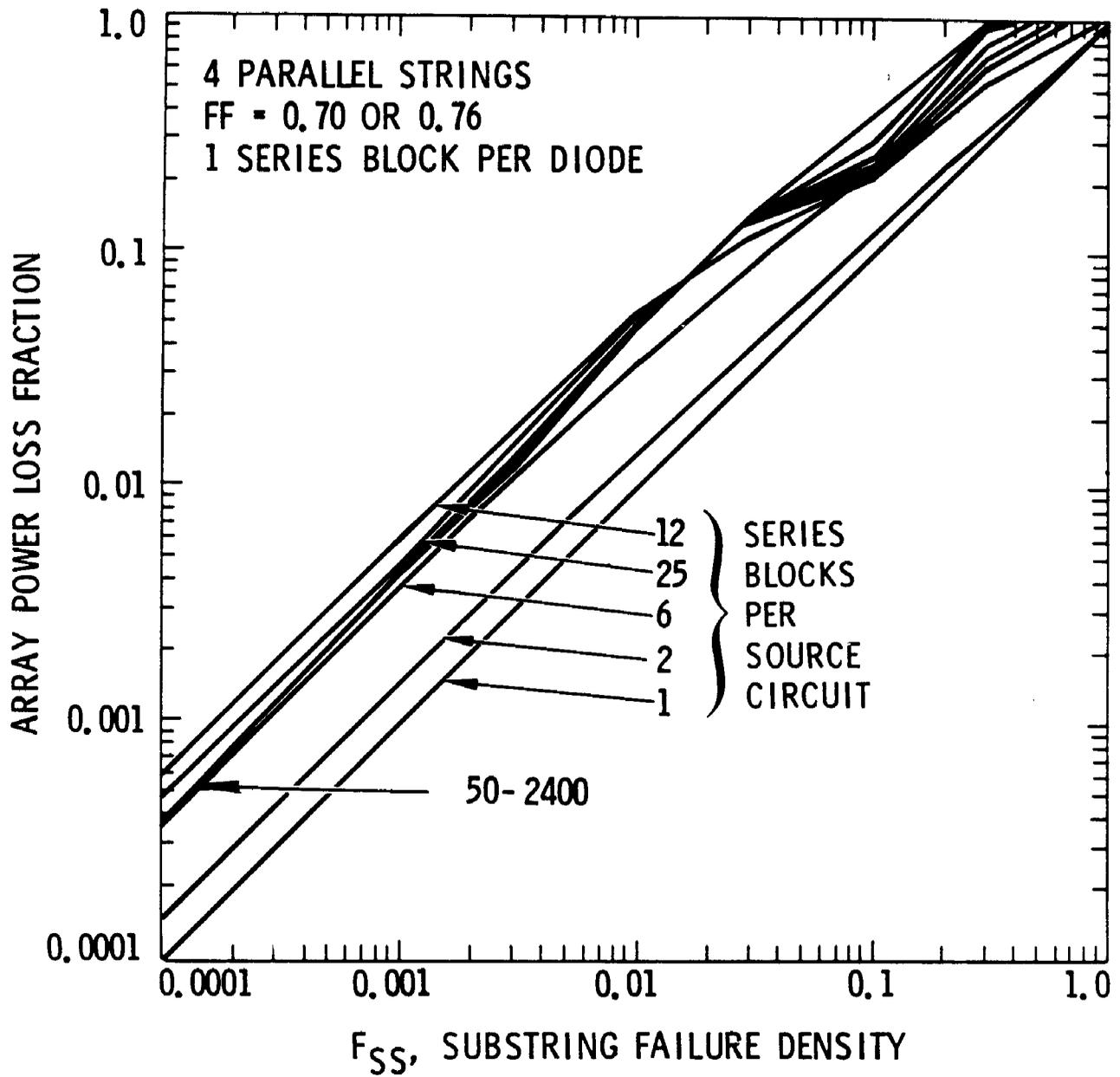
Each graph contains a number of separate curves, one for each of a variety of different number of series blocks per source circuit. The parameter values associated with each graph and its location in this appendix are indicated below. For an explanation of the terms and symbols used here see both Figure 1 (p. 3) and the Glossary at the beginning of the report.

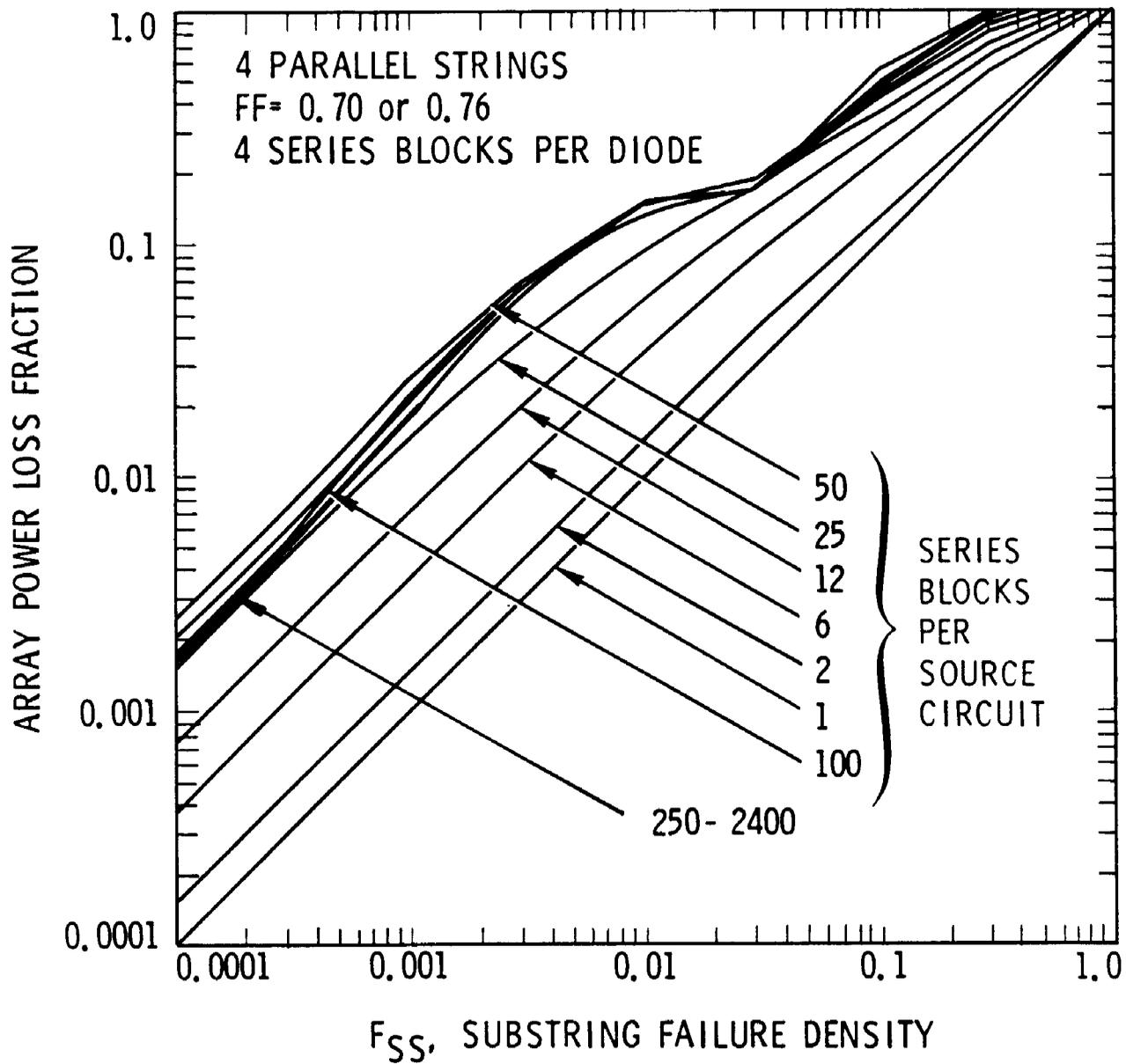
<u>No. of Parallel Strings</u>	<u>Fill Factor</u>	<u>No. of Series Blocks per Diode</u>	<u>Page Location</u>
1	.70	1	B-2
4	.70	0	B-3
4	.76	0	B-4
4	.70 or .76	1	B-5
4	.70 or .76	4	B-6
4	.70 or .76	8	B-7
4	.70 or .76	12	B-8
8	.70	0	B-9
8	.70	1	B-10
8	.70	4	B-11
8	.70	8	B-12
8	.70	12	B-13
8	.76	0	B-14
8	.76	1	B-15
8	.76	4	B-16
8	.76	8	B-17
8	.76	12	B-18
16	.70	0	B-19
16	.70	1	B-20
16	.76	0	B-21
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16	.76	4	B-23
16	.76	8	B-24
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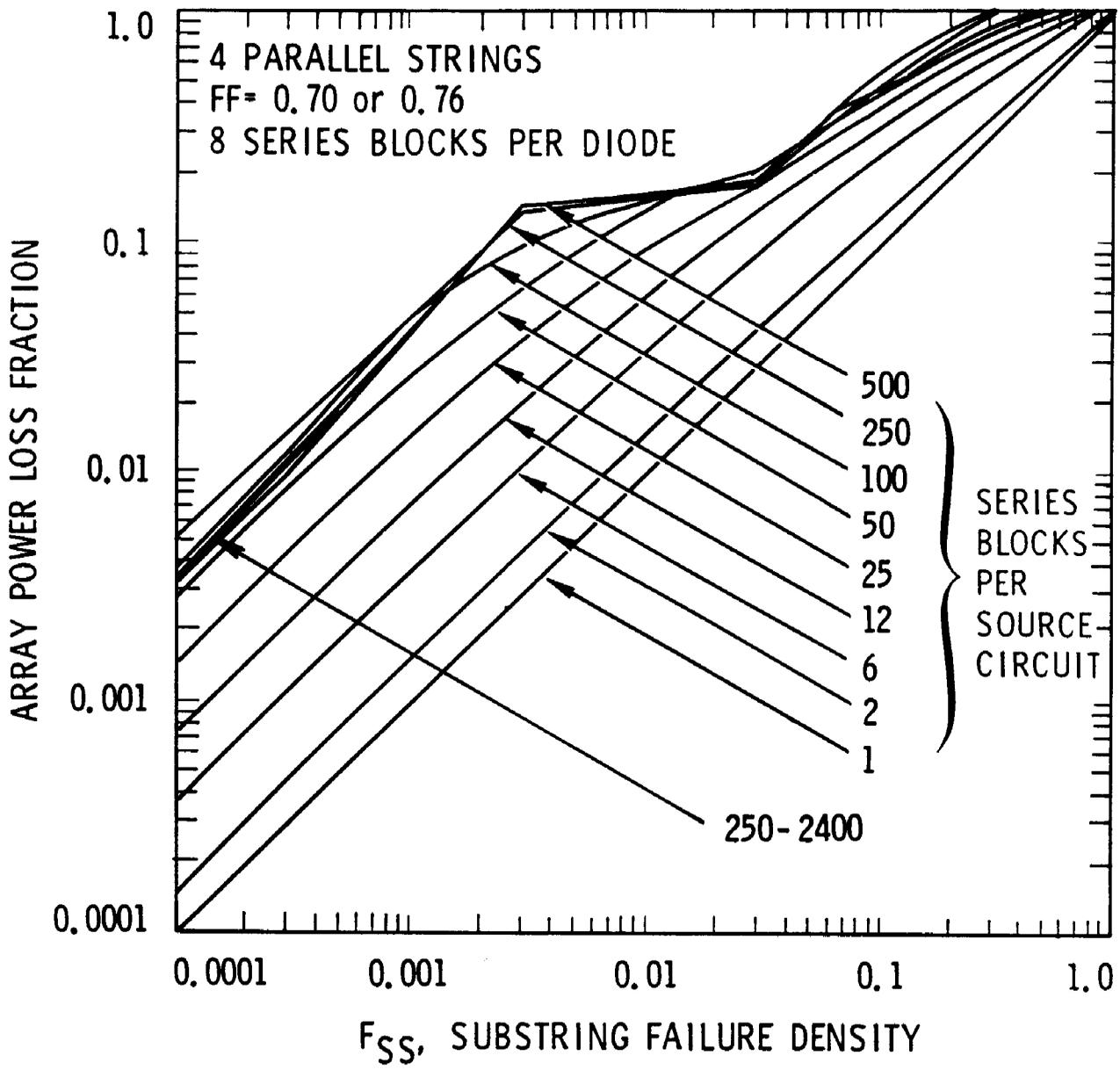


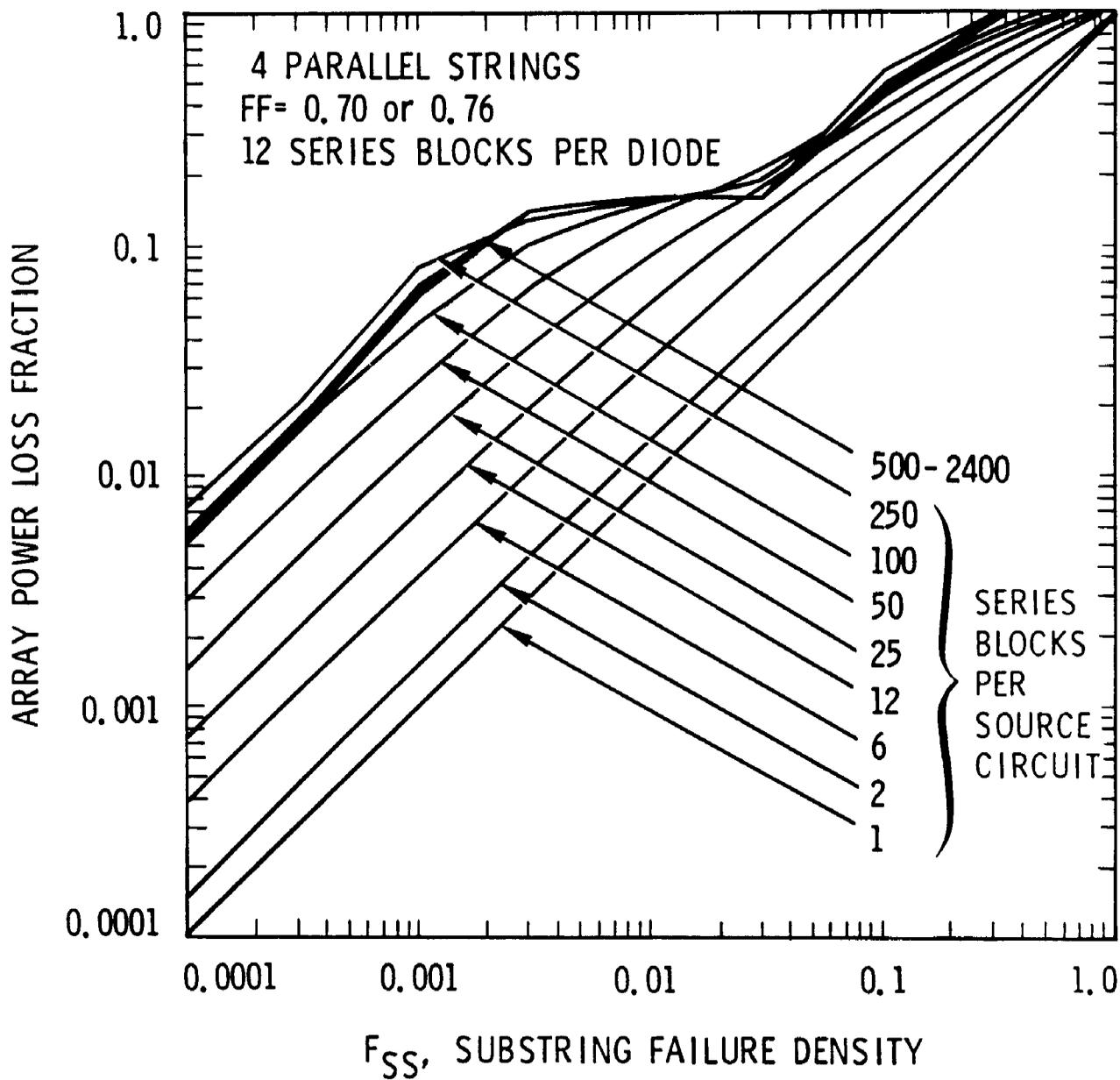


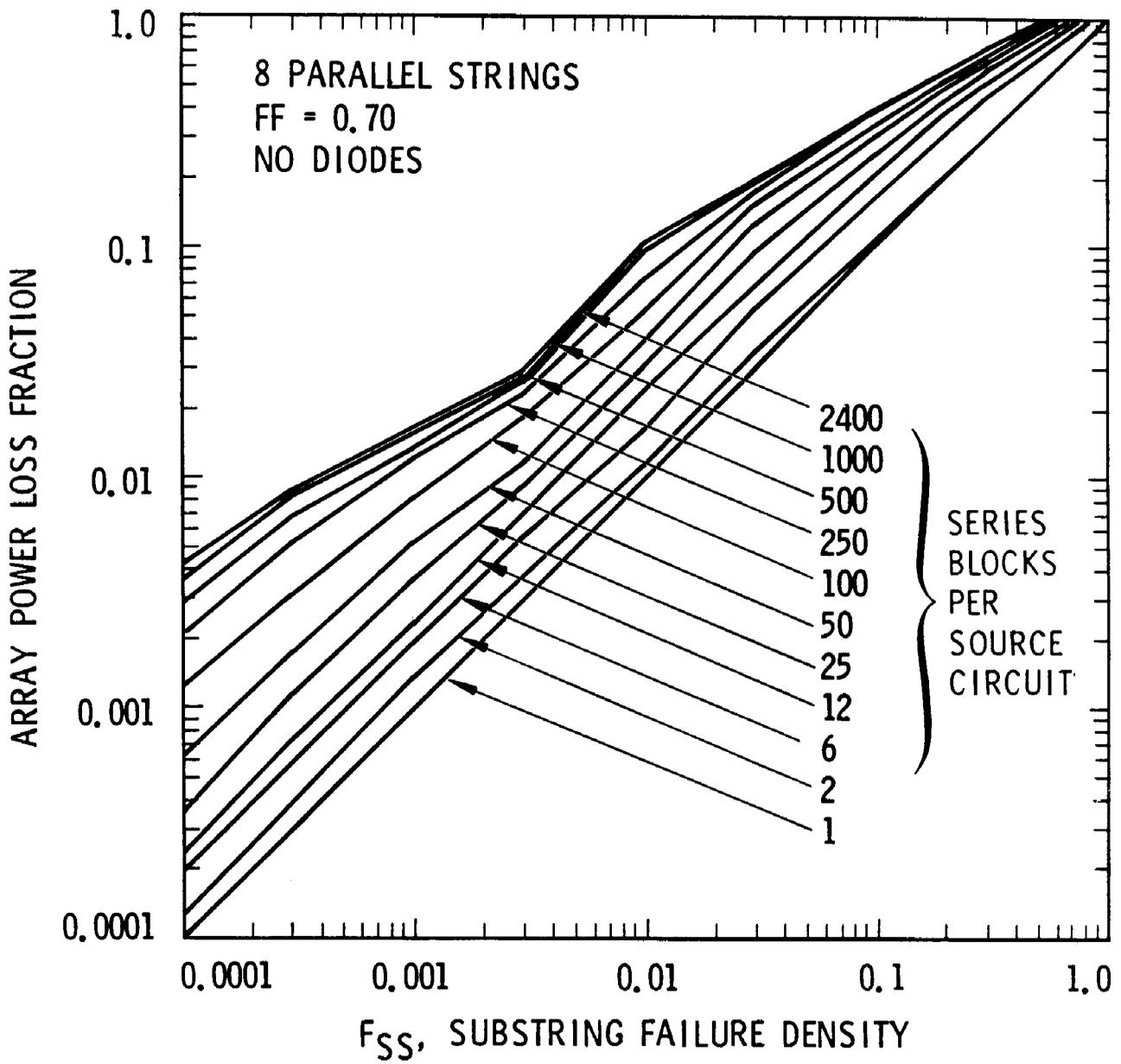


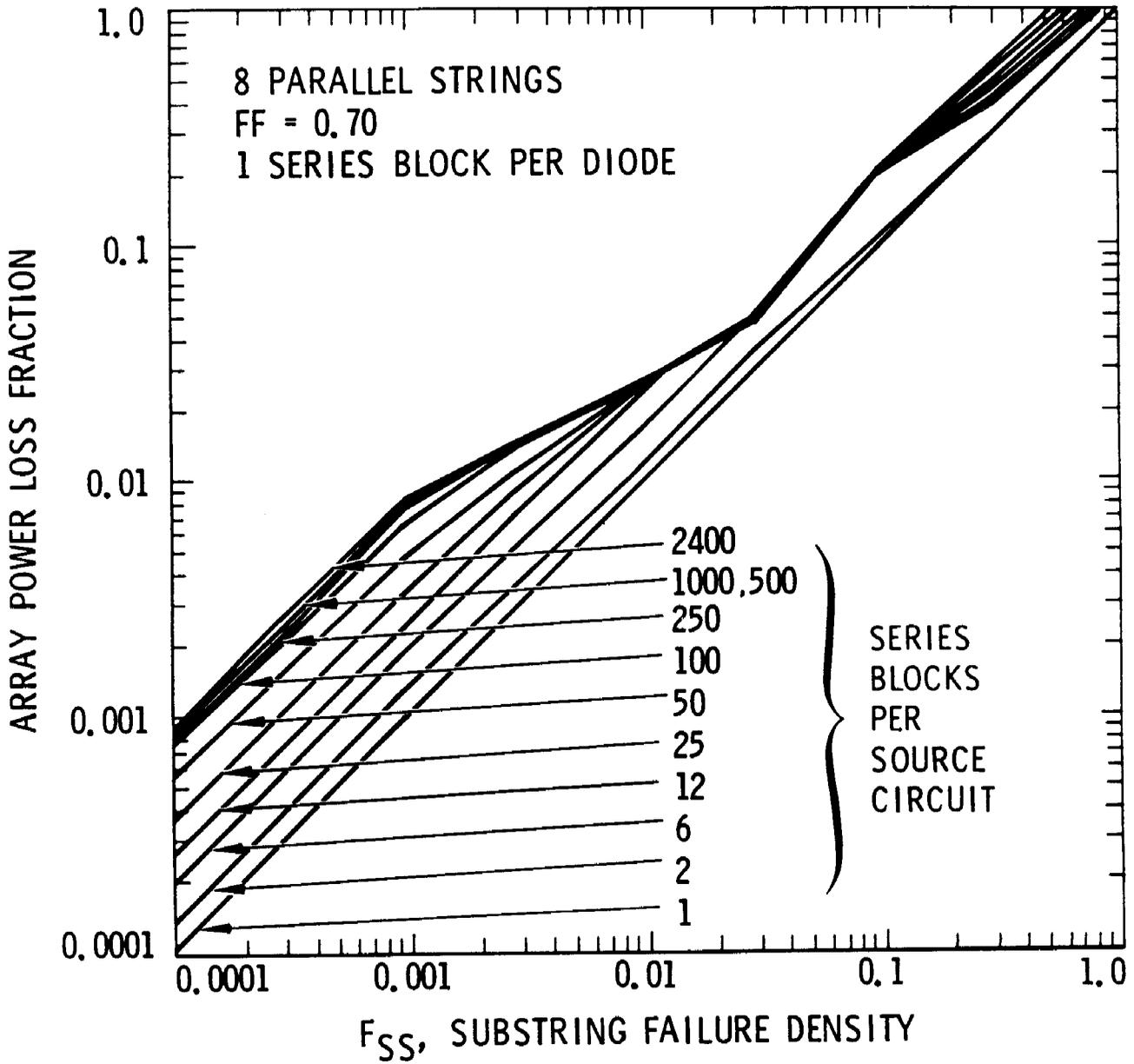


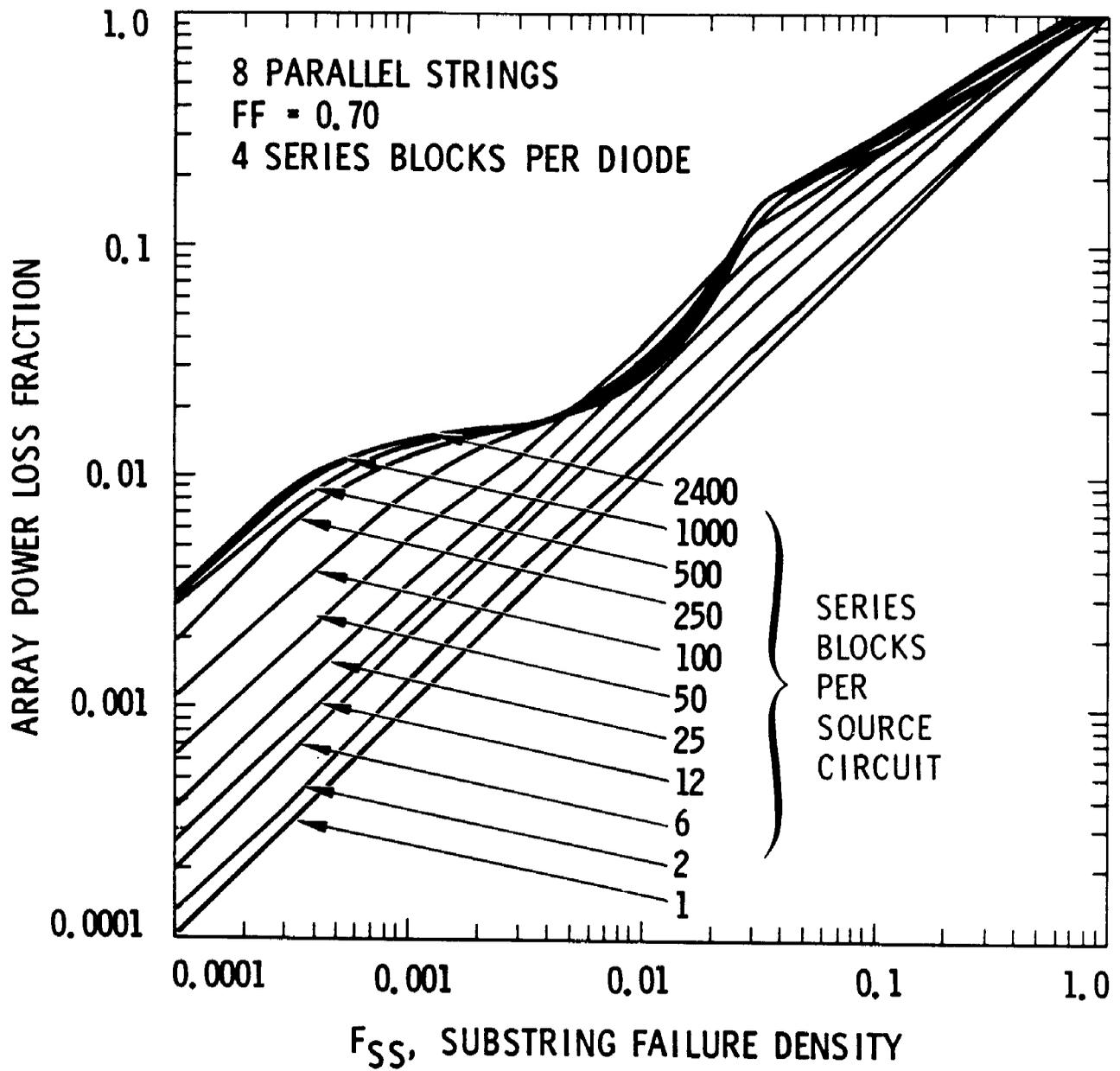


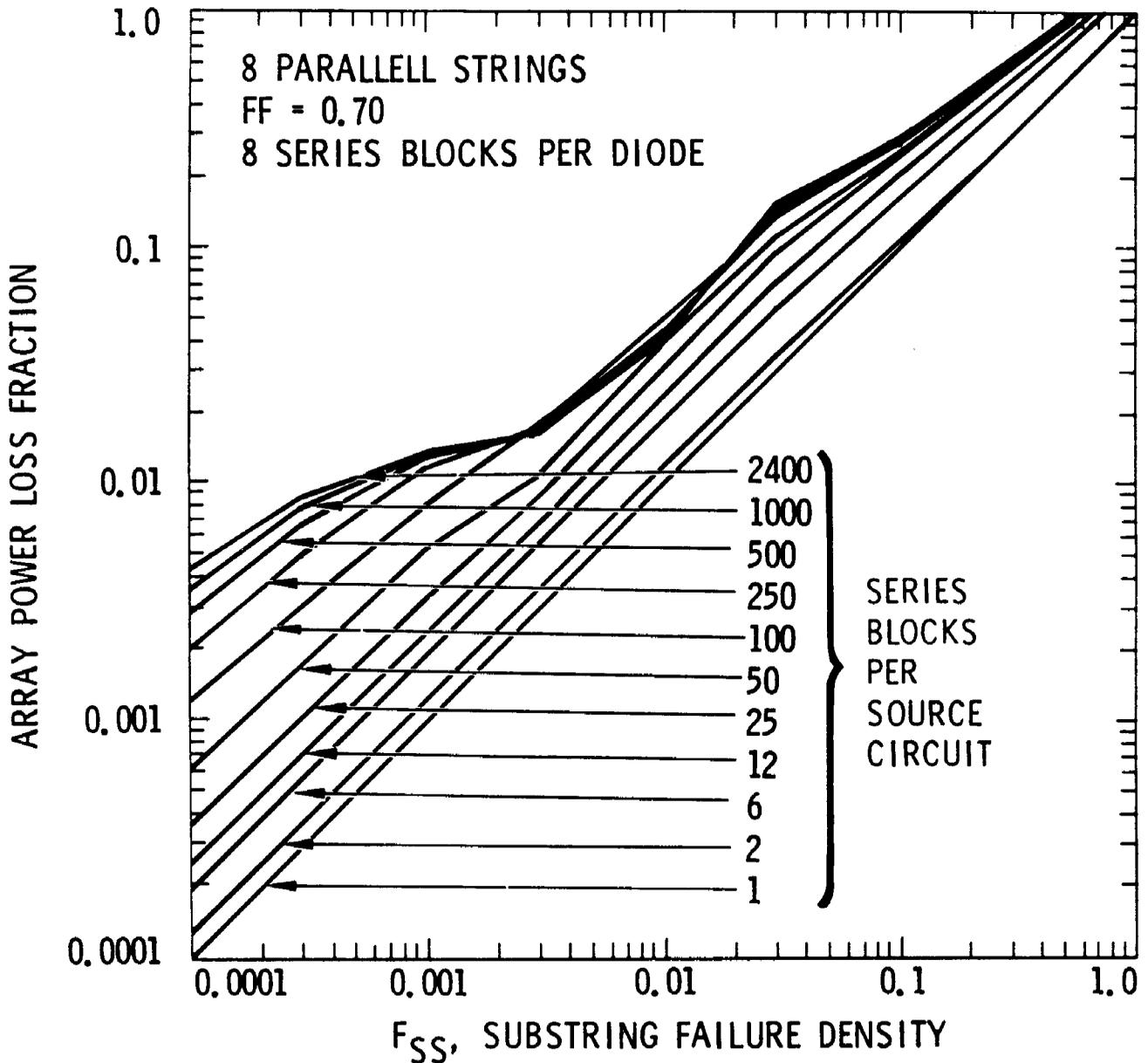


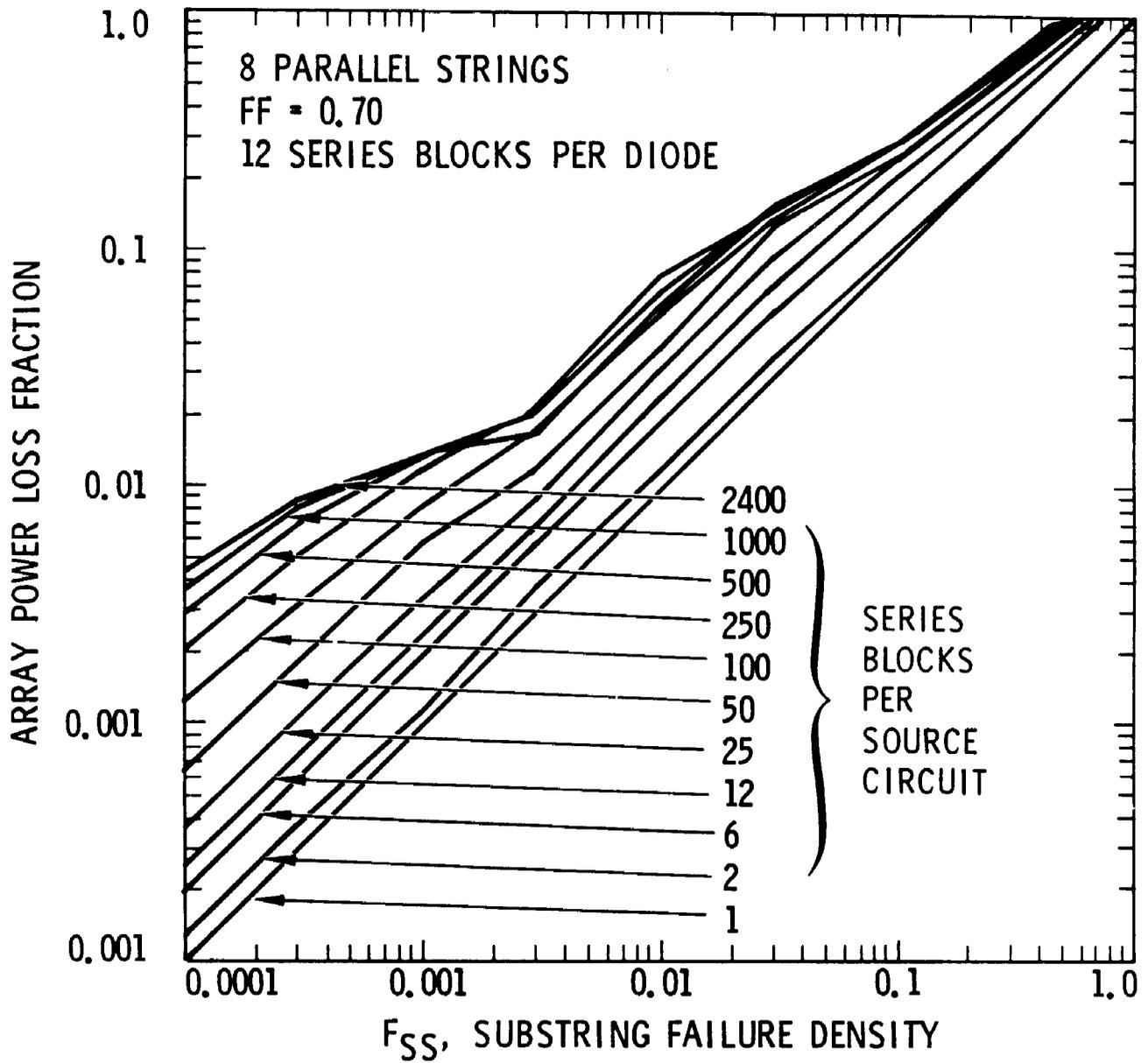


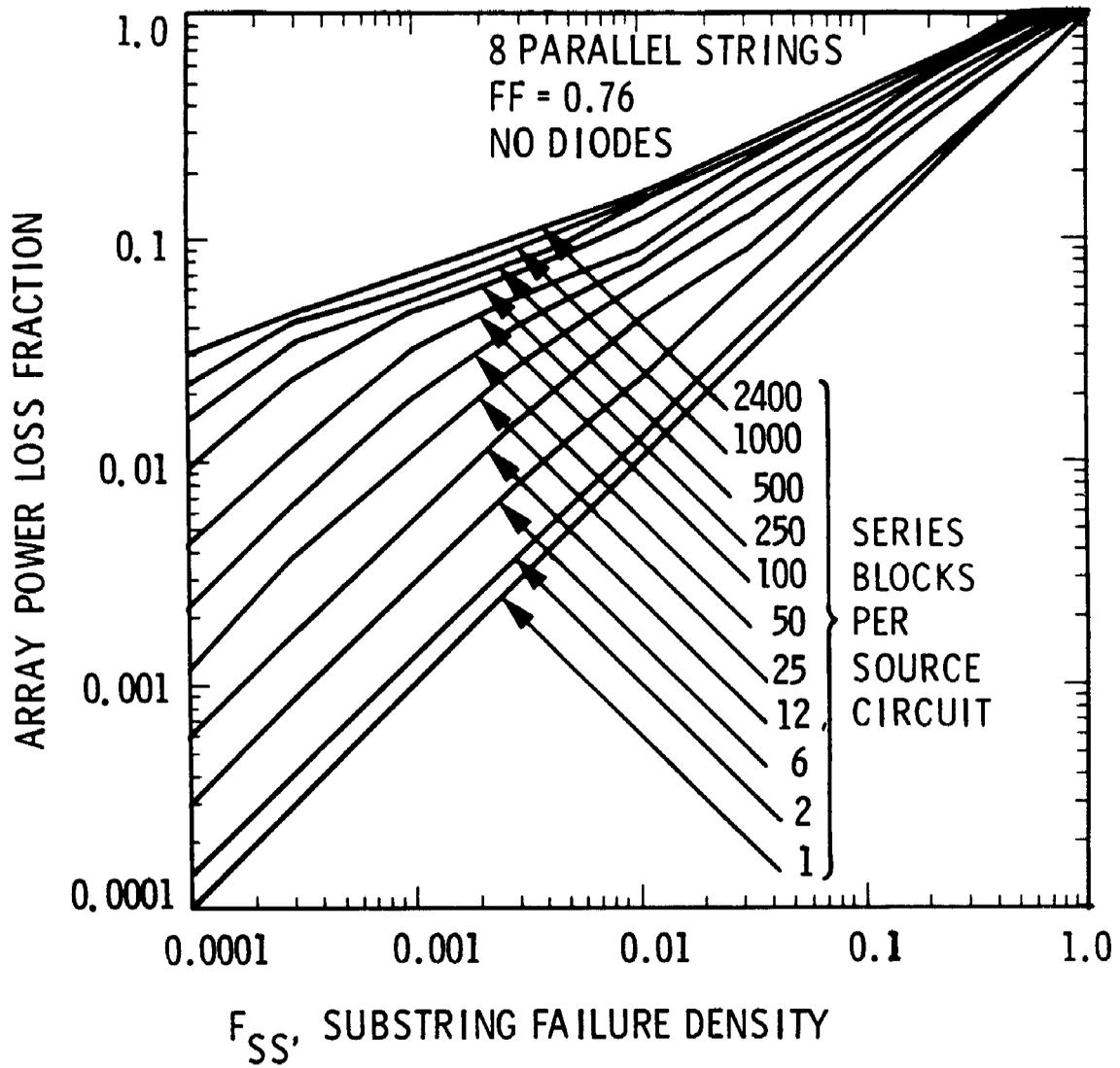


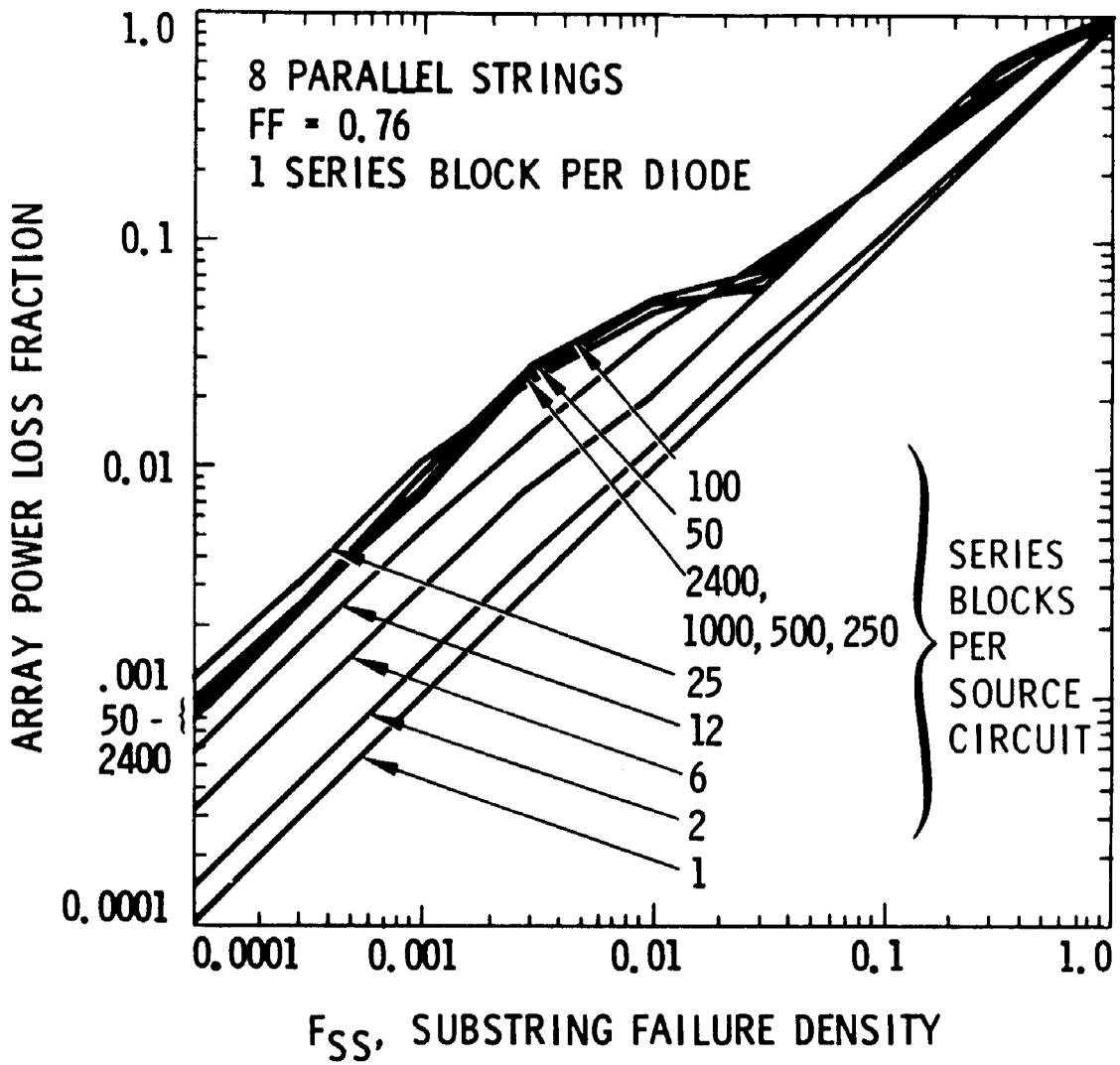


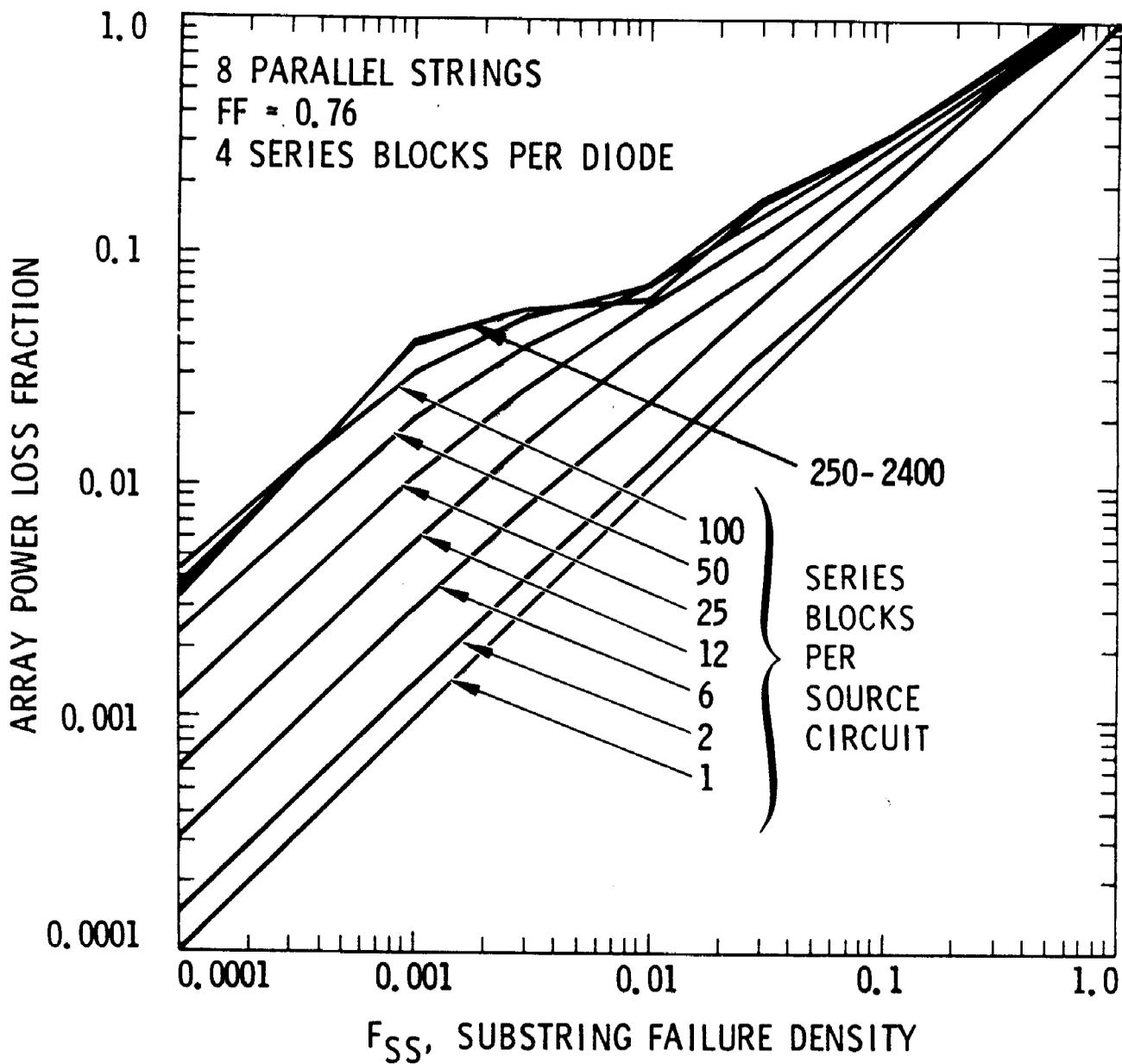


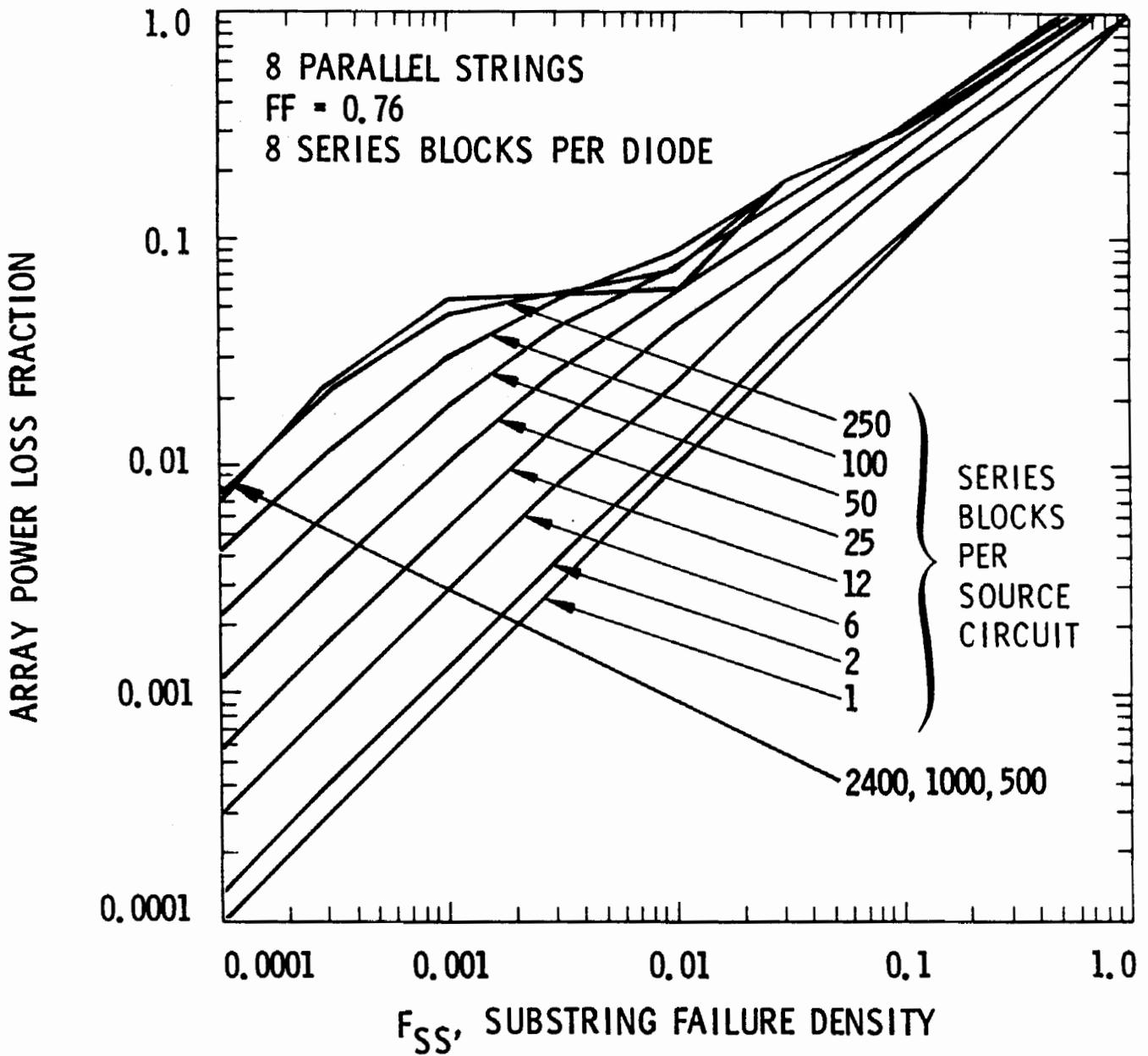


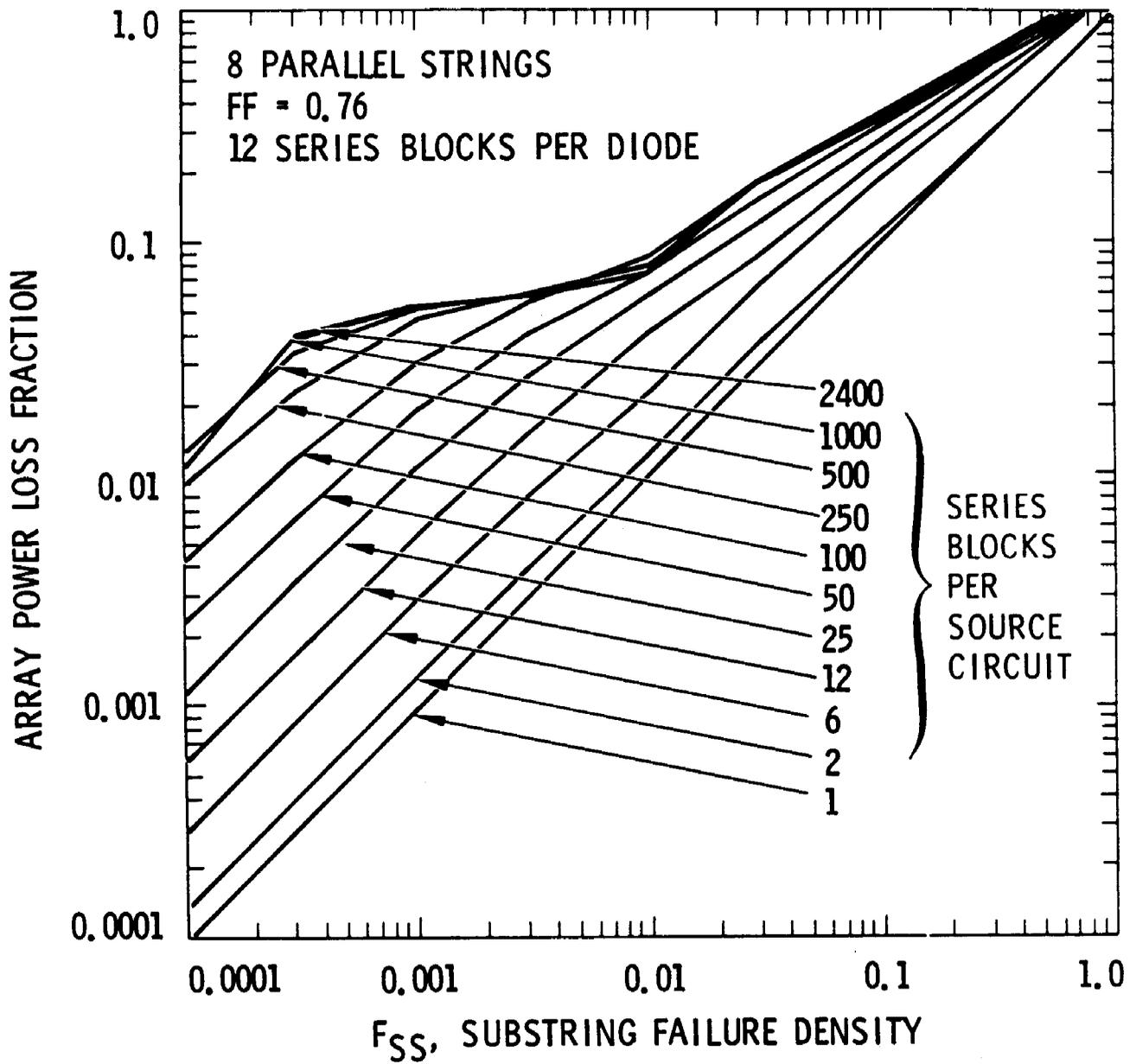


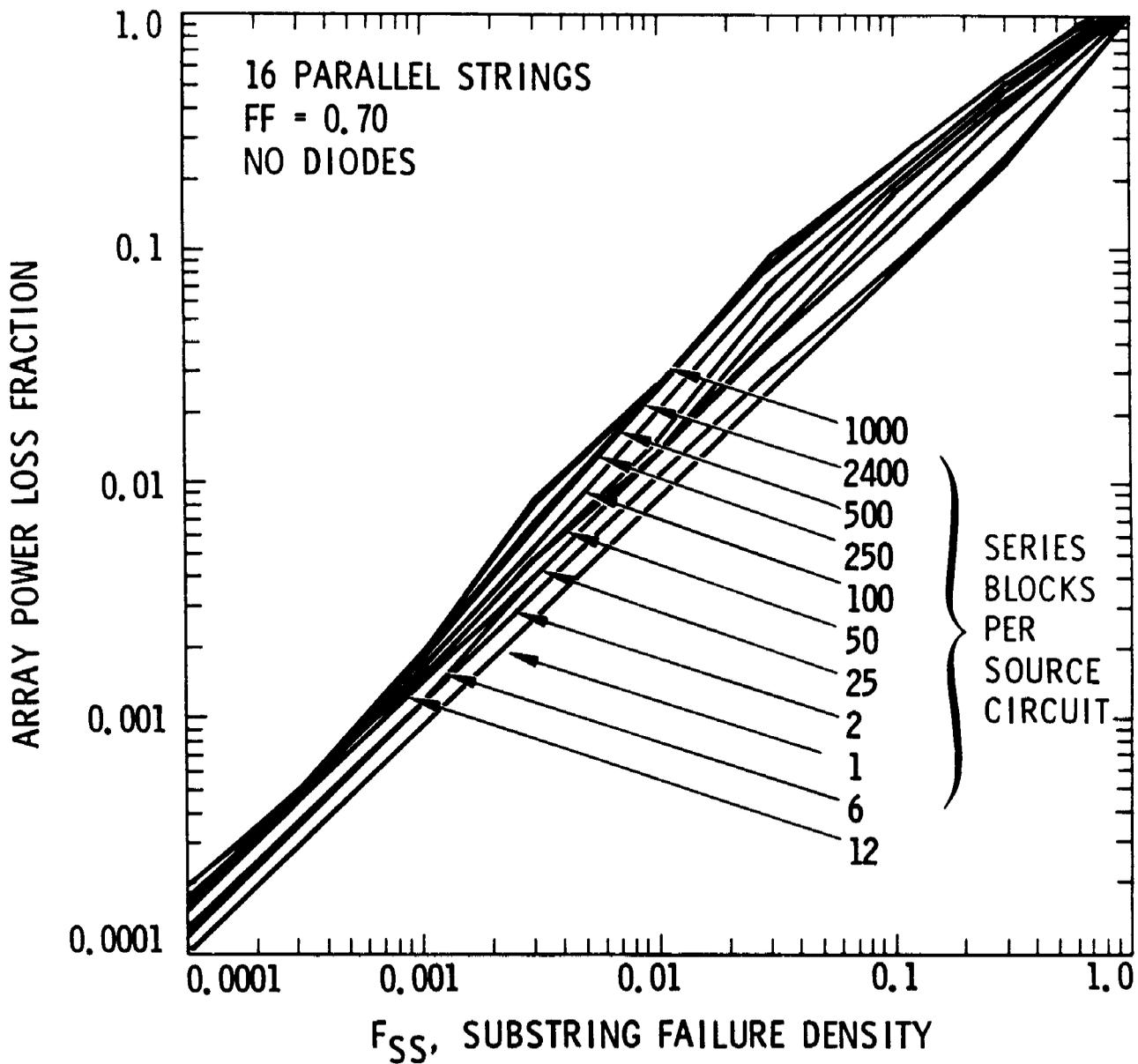


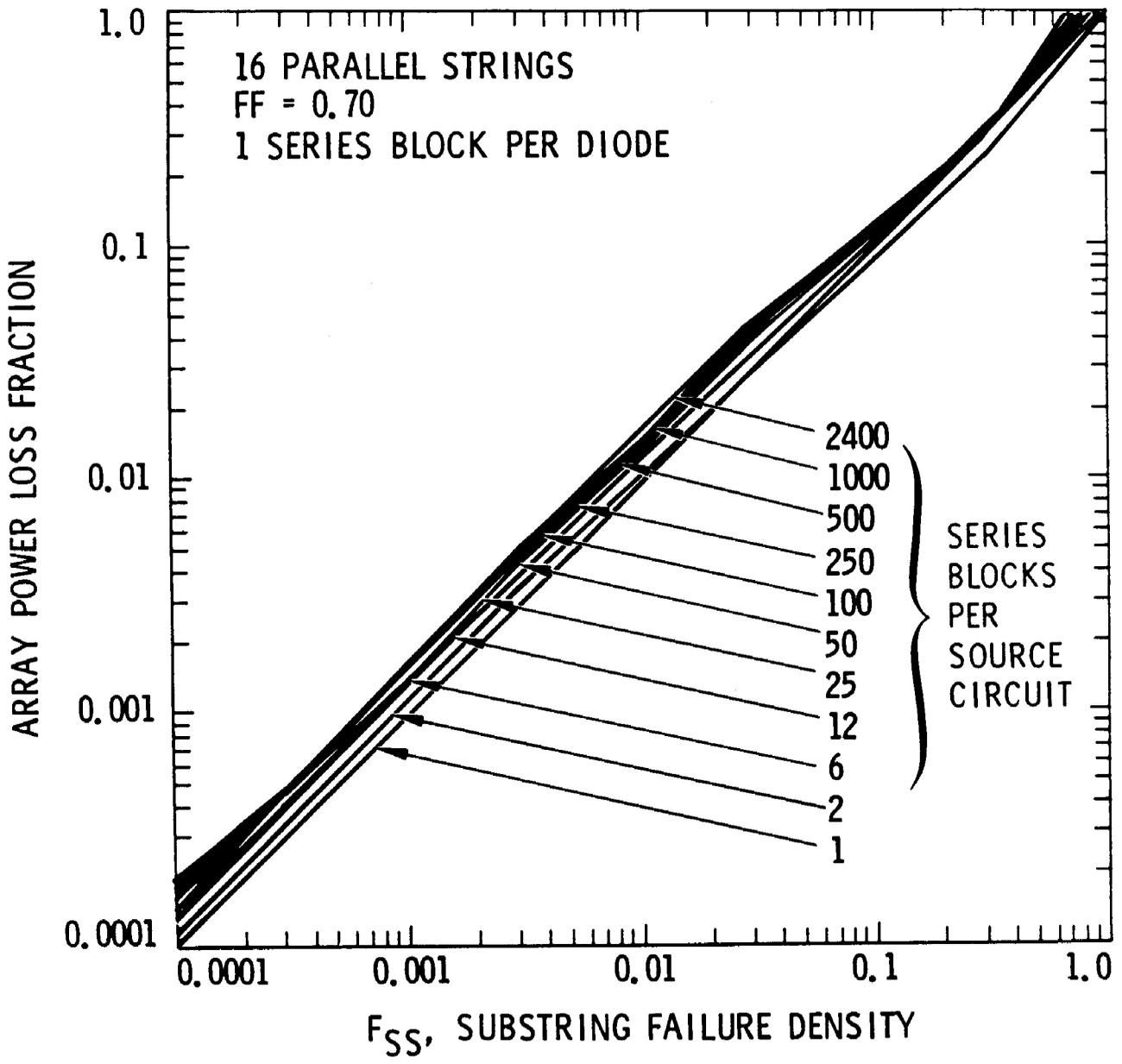


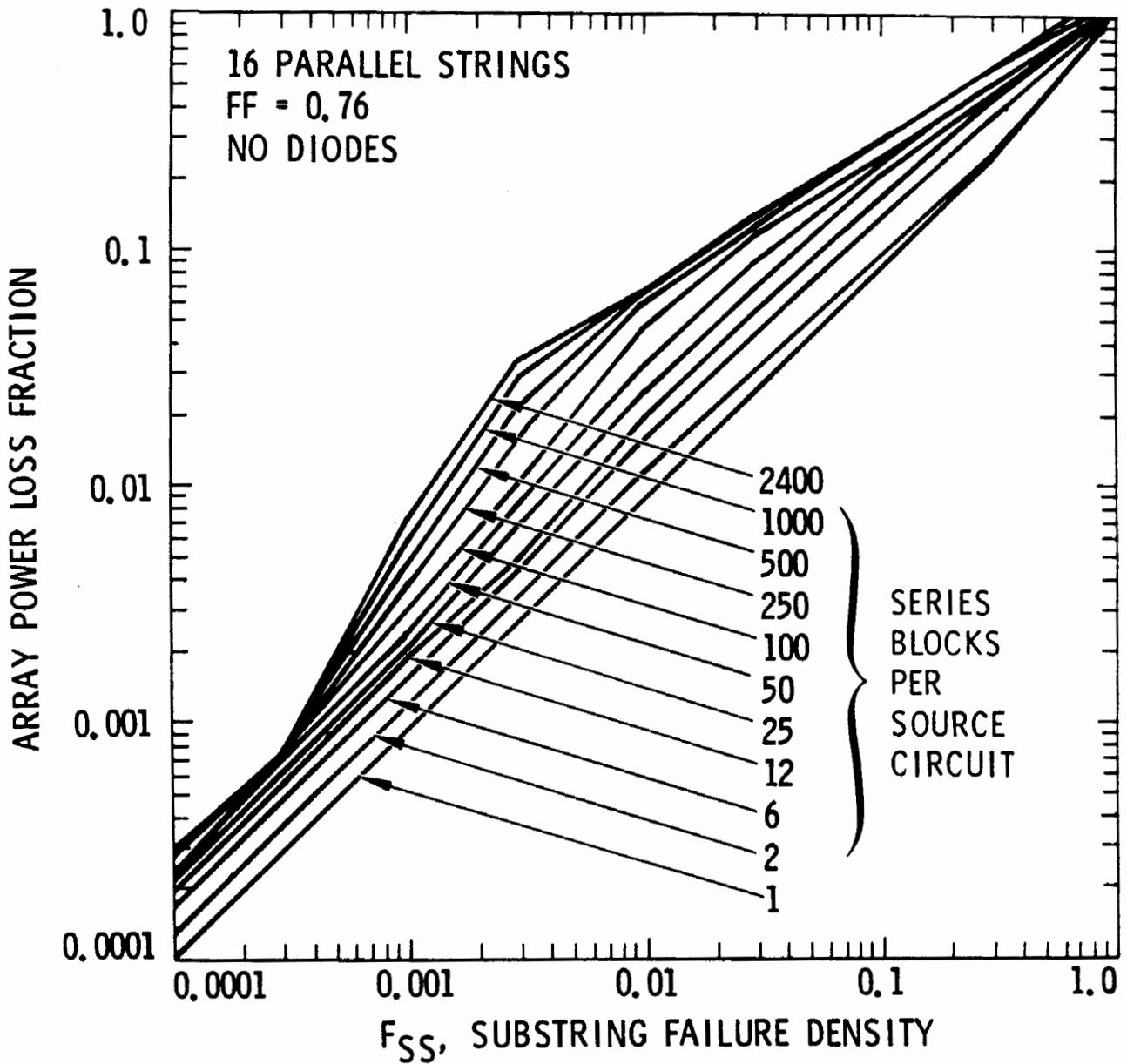


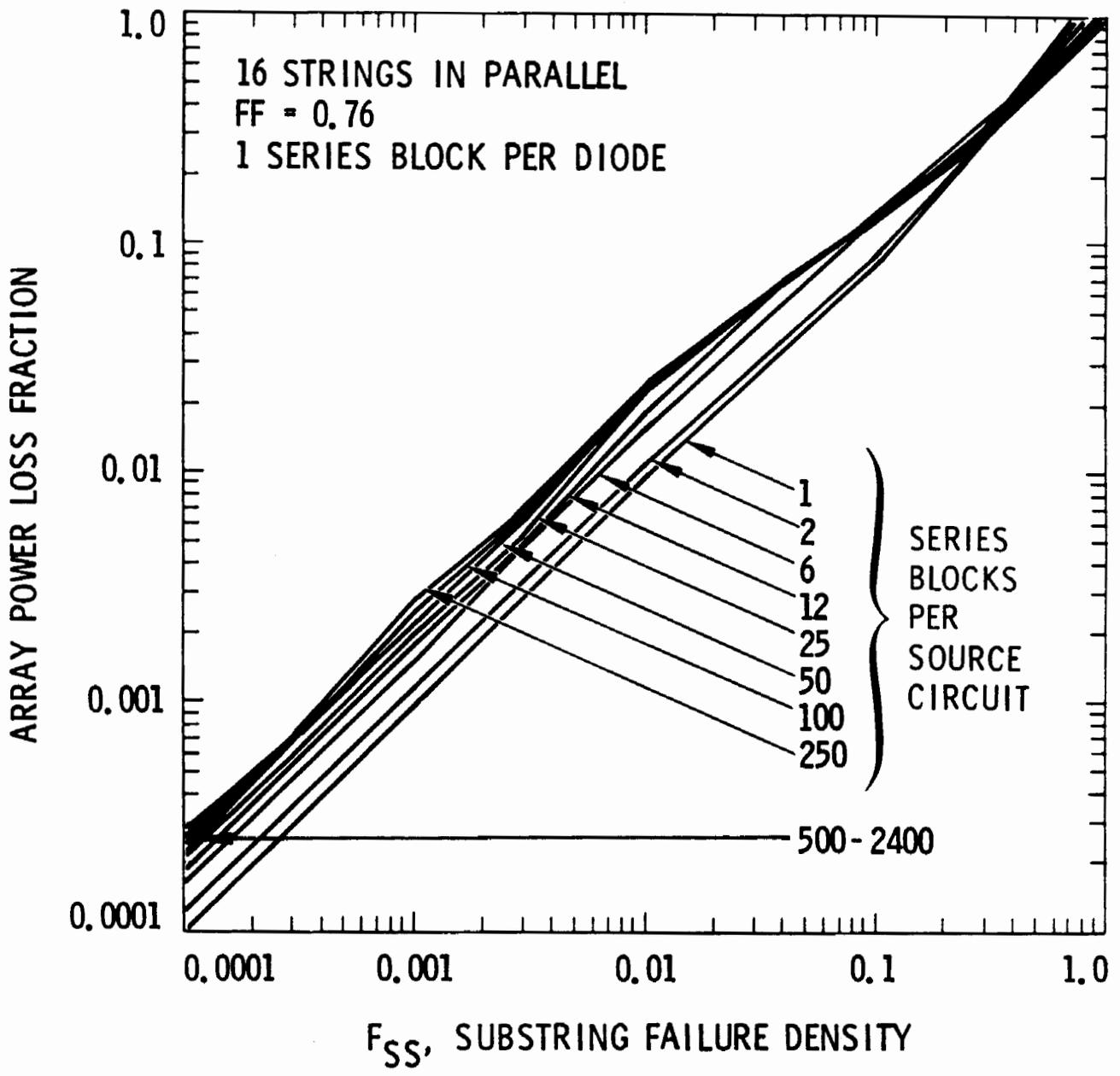


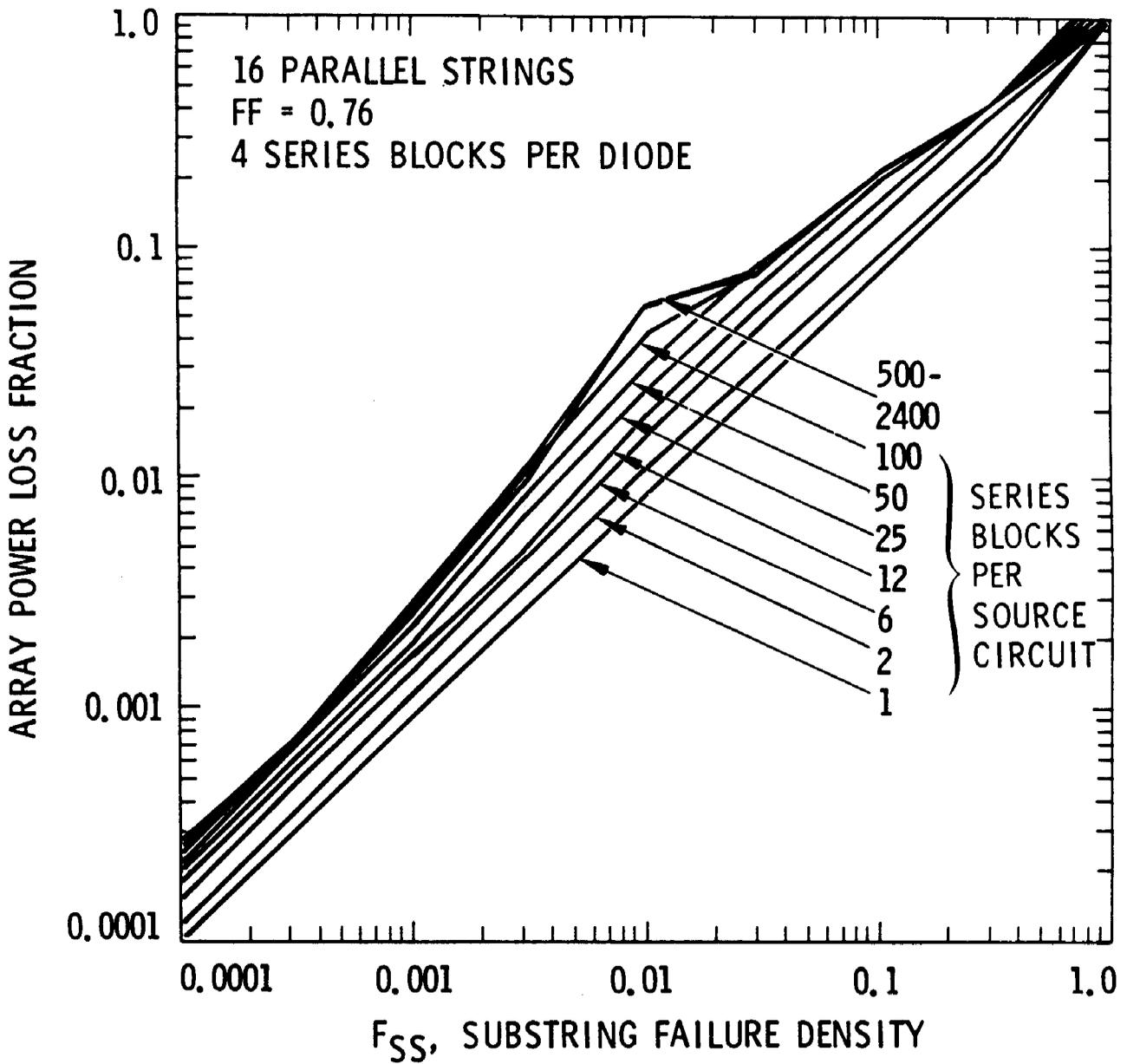


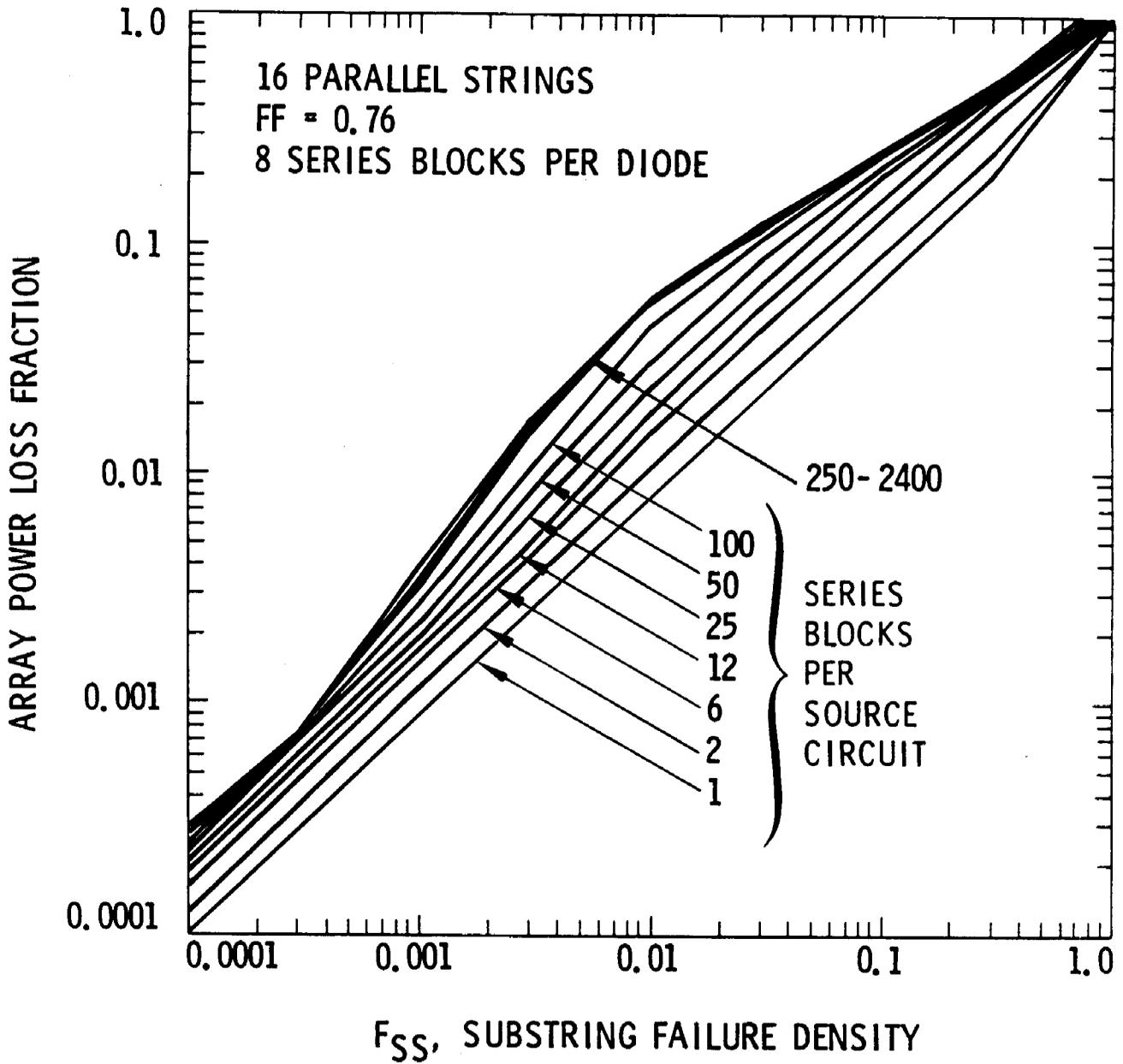


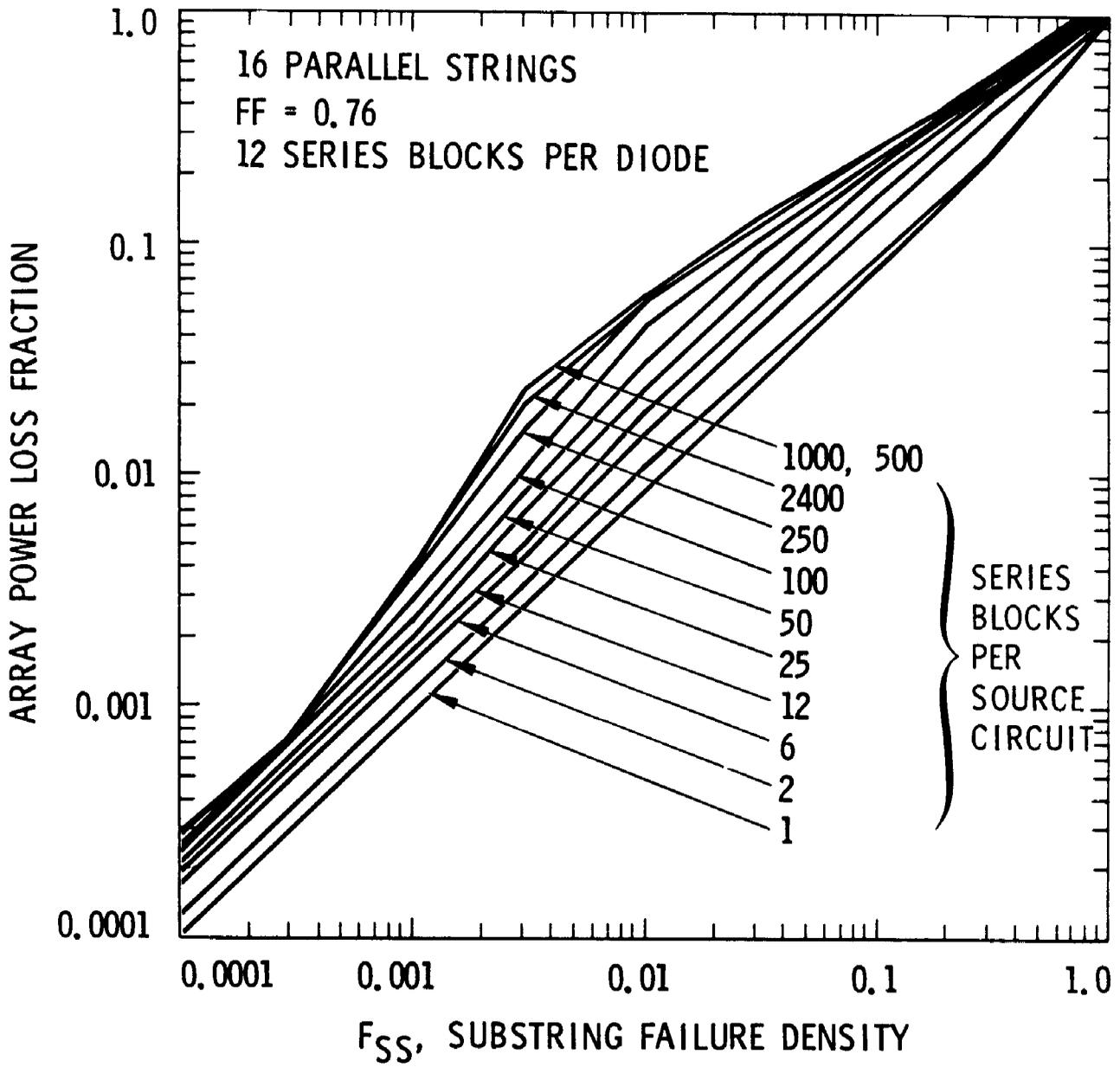












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