Reliability of photovoltaic modules*

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Abstract

As part of the U. S. National Photovoltaic Program, the Jet Propulsion Laboratory's (JPL's) Flat-Plate Solar Array (FSA) Project has conducted a comprehensive 10-year research activity addressed to understanding the reliability attributes of terrestrial flat-plate photovoltaic modules, and to developing the technology required to achieve 30-year life (1). This paper provides an overview of the reliability issues and progress, and highlights the design, analysis, and test tools generated to achieve the high levels of reliability necessary for future large-scale terrestrial applications. Much of the technology is also directly applicable to the large space arrays currently under consideration for use in extraterrestrial applications.

Introduction

The reliability of photovoltaic solar arrays is probably second in importance only to cost in the list of factors influencing the market acceptance of this new technology. Because of their modular nature, photovoltaic arrays possess a higher than normal sensitivity to common-mode failures, but at the same time offer a wealth of redundancy options to increase reliability. Achieving the high reliability demanded by future large-scale application requires that these reliability design attributes be understood well and used effectively.

As a tool for managing module and array reliability development, the FSA Project has adopted a target for life-cycle reliability costs equivalent to 30 years with no significant array power degradation. Because small levels of degradation or replacement are economically justified, a typical array meeting the target life will last somewhat longer than 30 years to recapture the life-cycle costs associated with the gradual degradation expected (see Fig. 1). A convenient means for quantifying the life-cycle costs associated with reliability attributes is based on computing the break-even photovoltaic energy cost over the expected life of the application (2,3):

$$R = \frac{C_0 + \sum_{i=1}^{L} C_i M_i (1+k)^{-i}}{\sum_{i=1}^{L} E_i (1+k)^{-i}} \qquad (1)$$

where:
- R = Cost (worth) of energy (startup-year \$/kWh)
- E_i = Energy generated in year i (kWh)
- C_o = Initial plant cost (startup-year \$)
- C_i = Cost per module replacement action (startup-year \$/module)
- M_i = Number of modules replaced in year i
- k = Present-value discount rate
- L = Plant lifetime (years)

Notice that the above expression explicitly includes the effects of array degradation versus time (E_i), module initial cost (C_o), and the cost of module replacement ($C_i M_i$).

In assessing the implications of the 30-year equivalent-life target, it is instructive to examine the life-cycle cost impact of typical failure modes found in present-day PV modules. For some mechanisms, such as front-surface soiling, the economic impact is directly proportional to the degradation level and is easily calculated. For others, such as open-circuit or short-circuit failures of individual solar cells, complex statistical-economic analyses that include the effects of circuit redundancy, maintenance practices, and life-cycle costing are required (3,5). Without such analyses, failure levels cannot be interpreted with meaning. Table 1 lists 13 principal failure mechanisms associated with modules made with crystalline-silicon solar cells. The units of degradation listed in the third column provide a convenient means of quantifying the failure levels of the individual mechanisms according to their approximate time dependence. For example, units of \$/yr in the context of component or module failures reflect a constant percentage of components failing each year. For components that fail with increasing rapidity (%/yr^2) is the unit used to indicate linearly increasing failure rate. For those mechanisms classified under power degradation, the %/yr units refer to the percentage of power reduction each year.

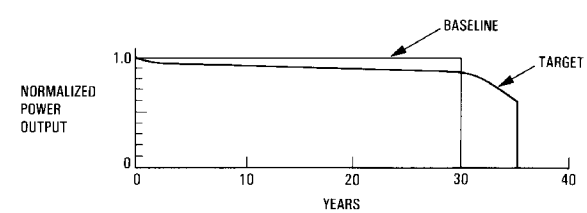

Figure 1. Typical target allocation for Time-Dependent Power Degradation.

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Table 1. System life-cycle energy cost impact and allowable degradation levels for 13 principal failure mechanisms for crystalline-silicon PV modules.

Type of Degradation	Failure Mechanism	Units of Degrad.	Level for 10% Energy Cost Increase* k = 0	k = 10	Allocation for 30-year Life Module	Economic Penalty
Component failures	Open-circuit cracked cells	%/yr	0.08	0.13	0.005	Energy
	Short-circuit cells	%/yr	0.24	0.40	0.050	Energy
	Interconnect open circuits	%/yr^2	0.05	0.25	0.001	Energy
Power degradation	Cell gradual power loss	%/yr	0.67	1.15	0.20	Energy
	Module optical degradation	%/yr	0.67	1.15	0.20	Energy
	Front surface soiling	%	10	10	3	Energy
Module failures	Module glass breakage	%/yr	0.33	1.18	0.1	O&M
	Module open circuits	%/yr	0.33	1.18	0.1	O&M
	Module hot-spot failures	%/yr	0.33	1.18	0.1	O&M
	By-pass diode failures	%/yr	0.70	2.40	0.05	O&M
	Module shorts to ground	%/yr^2	0.022	0.122	0.01	O&M
	Module delamination	%/yr^2	0.022	0.122	0.01	O&M
Life-limiting wearout	Encapsulant failure due to loss of stabilizers	Years of life	27	20	35	End of life

*k = Discount rate

Table 2. System life-cycle energy cost impact and allowable degradation levels for 13 principal thin-film module failure mechanisms.

Type of Degradation	Failure Mechanism	Units of Degrad.	Level for 10% Energy Cost Increase* k = 0	k = 10	Allocation for 30-Year-Life Module	Economic Penalty
Component failures	Open-circuit between cells	%/yr	0.08	0.13	0.02	Energy
	Short-circuit cells	%/yr	0.24	0.40	0.05	Energy
Power degradation	Light induced effects	%	10	10	5	Energy
	Cell gradual power loss	%/yr	0.67	1.15	0.20	Energy
	Module optical degradation	%/yr	0.67	1.15	0.02	Energy
	Front surface soiling	%	10	10	3	Energy
Module failures	Module glass breakage	%/yr	0.33	1.18	0.1	O&M
	Module open circuits	%/yr	0.33	1.18	0.1	O&M
	Module hot-spot failures	%/yr	0.33	1.18	0.1	O&M
	Bypass diode failures	%/yr	0.70	2.40	0.05	O&M
	Module shorts to ground	%/yr^2	0.022	0.122	0.01	O&M
	Module delamination	%/yr^2	0.022	0.122	0.01	O&M
Life-limiting wearout	Encapsulant failure due to loss of stabilizers	Years of life	27	20	35	End of life

*k = Discount rate

Using the units described above, Columns 4 and 5 of Table 1 indicate the level of degradation for each mechanism that will results in a 10% increase in the cost of delivered energy from a large PV system. Because the mechanisms will generally occur concurrently, the total cost impact is the sum of the 13 cost contributions. Column 6 lists a strawman allocation of allowable degradation among the 13 mechanisms to achieve a specific total reliability performance. In this case, the reliability allocations are consistent with a 20% increase in the cost of energy over that from a perfect, failure-free system with a 30-year life.

In contrast to Table 1, Table 2 provides similar data generated for 13 failure mechanisms likely to be associated with thin-film amorphous-Si cells monolithically deposited on a glass superstrate (4). Note that the module-failure and power-degradation mechanisms are essentially the same as those for crystalline-Si except for module optical degradation and light-induced effects. Because the thin-film cells are assumed deposited directly on the glass superstrate, there is no polymer in the optical path to the cell that can degrade in its transmission properties; the allocation for this mechanism is therefore substantially reduced. In its place is the new, and probably larger power degradation mechanism referred to as light-induced effects. The 5% allocation for this degradation assumes it reaches equilibrium quickly in the first few months of field application and remains constant at the 5% level over the plant life.

Although different degradation allocations could have been chosen in Tables 1 and 2, the important point is that these allocations allow the significance of observed failures to be measured, and goals to be developed to guide mechanism-specific research activities. The remainder of the paper addresses each category in light of the historical experience to date, and summarizes the technologies developed to achieve the listed allocations.

Component failures

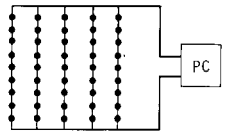
In the first category, titled "component failures", are cell-level failure mechanisms associated with open-circuiting or short-circuiting of individual solar cells. With crystalline-silicon devices, these failures generally result from cell cracking and mechanical fatigue of the cell-to-cell metallic interconnects. With thin-film cells this failure category is principally associated with open-circuiting of the cell-to-cell monolithic interconnect due to corrosion. Both types of devices also experience periodic short circuits, though this failure mechanism is far less troublesome than the open circuits.

At the root of the high sensitivity to cell failures indicated in Tables 1 and 2 is the need to interconnect electrically thousands of nearly identical solar cells in series and parallel to achieve the voltage and current levels of the intended application. For example, a 150-volt residential array will require 300 to 400 series cells, and a 1500-volt central-station application will require 3000 to 4000. This large number of series elements makes an array extremely sensitive to infrequent open-circuit cell failures even when a high level of circuit redundancy is used.

Fig. 2 graphically illustrates this sensitivity by noting the effect of one cell failure per 10,000 per year on various system configurations. To control this exaggerated sensitivity at high voltage levels, extensive use of circuit redundancy techniques such as series/paralleling and bypass diodes is recommended (3,5).

Fault-tolerant circuit design

Before the degradation allocation associated with solar-cell failures can be addressed further, the influencing effects of the available circuit redundancy solutions must be considered. The first step toward circuit redundancy is generally associated with dividing the large matrix of cells that makes up the array into a number of parallel solar-cell networks referred to as source circuits. The source circuits provide convenient points for monitoring array performance and provide an ability to isolate small areas of the total array for maintenance and repair.



ARRAY VOLTAGE	SERIES CELLS (S)	POWER LOSS AT 5 YEARS
15	36	1.8%
150	360	16.5%
1500	3600	83.5%

POWER LOSS = 1 - $[1 - (\text{YEARS} \times R)]^S$

Figure 2. Array degradation for an open-circuit cell failure rate of 0.01% per year versus number of series-connected cells with no circuit redundancy.

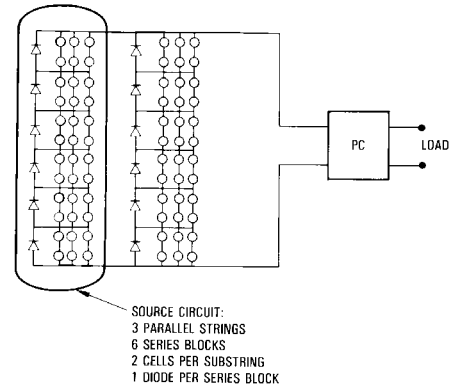


Figure 3. Series/parallel nomenclature.

As shown in Fig. 3, each source circuit may contain a single string of series solar cells or a number of parallel strings interconnected periodically by cross ties. The cross ties divide each source circuit into a number of series blocks. One or more series blocks may also be bridged by a bypass diode which is designed to carry the source-circuit current in the event that local failures constrict the current flow to the point of voltage reversal and power dissipation.

A key problem in assessing the impact of cell failures has been in quantifying the influence of specific series-parallel and bypass-diode arrangements on array degradation. This problem has been solved in recent years by the development of an extensive parametric analysis based on the statistical distribution of failed substrings due to random cell open-circuit failures (5,6). Reference 5 contains a large number of parametric plots, an example of which is shown in Fig. 4, which allows rapid computation of the effects of cell failures and circuit redundancy on array power loss.

Using these techniques, together with typical array and balance-of-system costs and efficiencies per reference (3), and a cell failure rate of 0.0001 per year, it is possible to calculate the break-even life-cycle energy costs for various redundancy and replacement options using Equation 1. Fig. 5 displays the calculated life-cycle energy costs for two replacement strategies as a function of the number of series blocks in source circuits composed of 8-parallel by 2448-series cells. In the first strategy, no module replacement is allowed and it can be seen that the life-cycle costs increase sharply with low numbers of series blocks. This reflects the rapid array degradation exhibited in Fig. 2 for series-string circuits without bypass diodes. For the second strategy (dashed curve) in Fig. 5, modules are replaced each time a solar cell fails during the 30-year life of the plant. This results in no power degradation, but does cause a substantial module replacement-cost contribution. This cost also varies with the number of series blocks due to improvements in module yield that occur when module series-paralleling achieves 8 parallel by 2 or more series blocks. This degree of module series-paralleling is only reached in this example when 272 or more series blocks are used per source circuit.

At this point, it is important to note that the economic impact of cell failures presented in Tables 1 and 2 assumes the high level of redundancy associated with the minimum life-cycle costs in Fig. 5. The critical question is therefore shifted to the feasibility of achieving the low cell-failure rates indicated as being necessary.

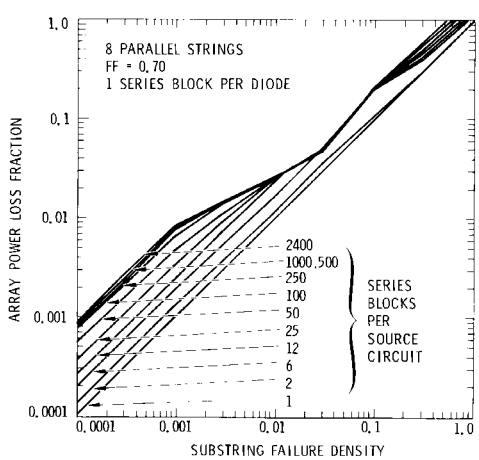


Figure 4. Example plot for power loss determination.

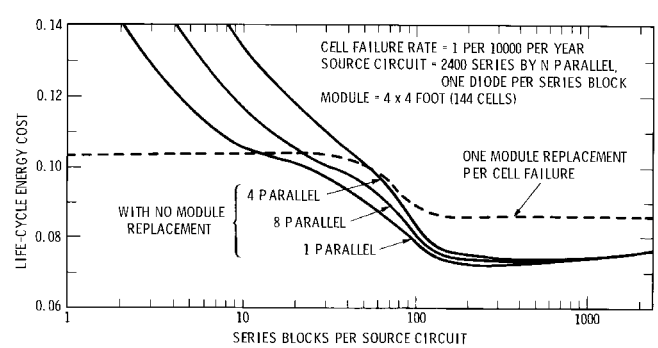


Figure 5. Relative life-cycle energy cost versus series/paralleling configuration and maintenance strategy.

For purposes of assessing this feasibility, a cell failure is considered as more than 25% degradation in short-circuit current compared with the average cell. This is generally sufficient to cause reverse biasing of the local bypass diode and therefore loss of power from the series block containing the failed cell.

Open-circuit cracked cells

Of the crystalline-Si cell-failure mechanisms seen in the field, cell cracking is probably the most prevalent. However, the number of cells with significant degradation (more than 25% degradation in short-circuit current) is very small, particularly with modern modules with high degrees of cell-contact redundancy. Most cracked cells remain electrically operative because the cell metallization and cell interconnects bridge the break and complete the electrical circuit.

Quantification of cell failure rates requires extensive and expensive auditing of the actual field performance of multikilowatt photovoltaic applications. Past audits of early crystalline-Si modules without modern contact redundancy, hail-impact resistance, or resistance to hot-spot heating indicated cell failure rates due to cracking at between 0.1% and 0.02% per year (5). The primary causes of cell cracking in the early applications appeared to be differential expansion between the cell and its support and impact loading by hailstones. The use of tempered glass superstrate design methods and thorough qualification testing (7) has vastly reduced the incidence of differential expansion and hail-impact damage; the introduction of multiple cell electrical contacts has similarly reduced the chance of a crack causing measurable electrical loss. Based on these improvements, it is estimated that current crystalline-Si cell failure rates are on the order of 0.001% per year, and therefore easily consistent with the needs expressed in Table 1.

Because of the manner in which thin-film cells are deposited on glass or stainless steel sheets, cell cracking has so far not been an issue with this technology.

Cell interconnects

Interconnect open-circuiting due to mechanical fatigue is an historical PV array failure mode that has been substantially eliminated in modern crystalline-Si modules. Like cell breakage, it is primarily caused by thermal and humidity expansion differences between the cell and its supporting substrate or superstrate. Mon, Moore, and Ross (8,9) have empirically characterized the fatigue-failure statistics of a variety of interconnect materials and geometries and have published detailed design methods for achieving optimal levels of interconnect reliability.

As with cell cracking, the solution is to design for very low numbers of failures (maybe 10% after 100 years) and then to incorporate interconnect redundancy to control power losses associated with those that fail.

From the empirical data, interconnects are found to fail with a log-normal distribution, with the weakest failing as much as 100 times sooner than the average. The low-probability tail of the distribution is well modeled as a linearly increasing failure rate. The levels indicated in Table 1 reflect easily achievable life-cycle optimums for doubly redundant interconnects, based on the work of the cited authors (9).

Unlike the wire interconnects used in crystalline-Si cells, thin-film solar cells, are often interconnected by careful overlapping and scribing of adjacent cell layers during module processing. This leads to a continuous monolithic interconnect from cell to cell, running along the long dimension of the narrow cells. Unfortunately open-circuiting of this monolithic interconnect has taken its toll in some early amorphous-Si field installations. The problem manifests itself during humidity testing and not during thermal cycling, and is associated with corrosion of the aluminum back metal in the region of the interconnects. Because of the high sensitivity to open-circuit cells noted in Table 2, this failure mechanism is actively being researched and solutions seem promising.

Power degradation mechanisms

In addition to the component statistical failure mechanisms discussed above, a variety of observed mechanisms typically lead to gradual degradation or loss of power over the life of a PV array. These generally fall into two categories: optical losses and cell power degradation. Both of these degradation modes tend to be generic as opposed to being statistical; i.e., the majority of modules and cells of the same type degrade at the same rate with little statistical scatter. Most systems must be designed to accommodate this gradual power decrease, as the only correction techniques involve incremental addition of array area or total module replacement.

Gradual power loss in cells

This category covers a variety of solar cell degradation mechanisms including increased series resistance, junction shunting, and deterioration of the cell antireflection (AR) coating. All of these mechanisms are found to some degree in both crystalline and thin-film modules.

Increased series resistance is often associated with a gradual deterioration of the adherence between the cell metallization and the cell bulk material due to corrosion-related processes, or the deterioration of the ohmic contact through the formation of a Schottky barrier. Junction shunting is caused by the diffusion or migration of metallization elements into the cell junction or over the external surfaces of the cell. The

third cell degradation mechanism relates to the deterioration of the AR coating on the solar cell's irradiated surface due to leaching or contamination from plating or corrosion products. All of these mechanisms lead to a gradual reduction in the cells electrical efficiency and are quite sensitive to the choice of metallization and AR-coating materials and processes. Work at Clemson University has shown that moisture and thermal aging are key environmental stresses, and that the module encapsulant system exacerbates the problem as often as it helps (10).

In all three mechanisms, the most effective techniques for quantifying expected levels of degradation involve accelerated temperature/humidity testing together with Arrhenius plotting and other means of relating the data to long-term use conditions (10,11,12). Experience gained through the extensive testing of Crystalline-Si cells and modules (10,12) suggests that the best present-day modules of this type are quite consistent with the 0.2%/yr power-degradation goal proposed in Table 1. However, reflecting their early stage of development, first generation thin-film modules have been found to be quite sensitive to these corrosion-related mechanisms; corrosion-resistant designs are actively under development to meet the goals of Table 2.

Light-induced effects

Light-induced effects is the name associated with a class of degradation mechanisms principally associated with thin-film amorphous silicon solar cells. The phenomena is caused by a light-induced degradation of the semiconductor properties of the cell and is manifested as a degradation in the current-voltage performance of the cell. As noted in Fig. 6, the degradation proceeds rapidly upon first exposure of the cell to light, and then gradually reaches a stable equilibrium with time. The rate and degradation is quite sensitive to the illumination level and to the cell electrical loading point (short circuit versus open circuit) during the aging process (14,15). Because the light-induced degradation is often on the order of 30 to 50%, this mechanism is the subject of extensive ongoing research.

Module optical degradation

Aside from external surface soiling, discussed in the next subsection, module optical degradation is generally caused by encapsulant transmission loss in the form of uniform yellowing due to ultraviolet (UV) and temperature-induced self-degradation, or local yellowing due to foreign matter diffusing into the encapsulant; e.g., from edge seals, mounting hardware, and electrical-terminal hardware.

Substantial research has been done on these various degradation mechanisms over the past few years, and a variety of highly stable materials and additives have been identified (16, 17). Of key importance, in addition to starting with UV-resistant materials, is the proper incorporation of UV absorbers and antioxidants, and preventing their loss over time due to leaching and diffusion. Similarly, interfacing materials such as gaskets and electrical terminal hardware must be carefully chosen for chemical compatibility with the primary cell encapsulant (12).

As with the cell degradation mechanisms, the most effective techniques for quantifying expected levels of degradation involve carefully accelerated temperature-humidity and UV testing, together with various means of relating the data to long-term use conditions (11,12,18). A key factor in such testing is properly accelerating the mechanisms that cause loss of the stabilizing additives. Vented ovens and water sprays play an important role in this respect.

With modern encapsulants, such as highly stabilized ethylene vinyl acetate (EVA), proper choice of interfacing materials, and careful attention to preventing loss of the additives, it is expected that the 0.2% per year degradation rate listed in Table 1 is being achieved.

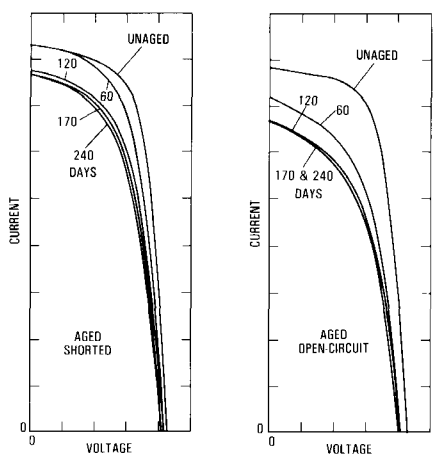


Figure 6. I-V performance degradation due to light induced effects versus outdoor aging period (ambient operating temperature).

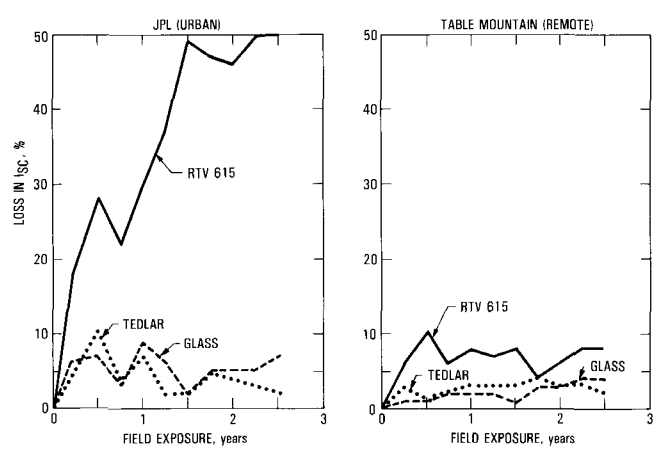


Figure 7. Loss in array short-circuit current (I_{SC}) due to soiling versus days of field exposure.

Front-surface soiling

Although similar in effect to other optical-loss mechanisms, experimental data indicate that optical surface soiling due to dust and atmospheric contaminants reaches equilibrium levels in a few weeks and then fluctuates somewhat with natural cleaning mechanisms such as rain. The net result is most easily modeled as a fixed loss in array current and power over the life of the array.

Figure 7 illustrates this soiling behavior for a variety of module surface materials in two site environments--one urban, the other remote. These and other data gathered by JPL during the past 6 years at a variety of sites in the United States indicate that average soiling levels below 5% should be easily achievable with glass or Tedlar-like optical-surface materials, without washing (19). Very dusty remote sites and heavily polluted urban sites will, of course, exceed these levels and may require periodic washing.

Module-failure mechanisms

In addition to component failures that are best treated at the cell level, a number of failures are more appropriately considered at the module level. These include glass breakage, electrical insulation breakdown, and various types of major encapsulant failure such as delamination. Like cell failures, these failures are also flaw-related and must be treated statistically when considering quantities of modules in a large array.

When designing for appropriate levels of module failures, it is important to note that a module failure is likely to cause an electrical hazard or major power loss and will therefore require immediate repair or replacement. As a result, module failure rates are traded off against life-cycle maintenance costs as opposed to redundancy and life-cycle energy loss, which are associated with cell failures.

Module glass breakage

With the extensive development of glass superstrate modules in recent years, many of the reliability problems of past module designs have been substantially solved. At the same time, however, glass breakage was introduced as a possible failure mechanism. Although vandalism is probably responsible for some glass breakage, other key causes include frame-induced thermal stresses, handling damage, wind loads, and hail impact.

Thermal-stress failures are generally caused by mounting untempered glass in a frame, which leads to the periphery of the glass heating more slowly than the center area when sunlight strikes the dark, absorbent solar cells. The expanding center places the flawed glass edges in tension, leading to mechanical stresses greater than that allowable for untempered glass. With its increased strength, tempered glass is easily able to withstand the thermal stresses, and provides an effective solution to the problem.

Substantial research has been conducted during the past few years to develop means of accurately predicting the breaking strength of glass subject to uniform pressure loads. Because glass fracture is dependent on the coincidence of a flaw and a high stress, glass strength varies widely from sheet to sheet and from location to location within a sheet. Based on a combination of nonlinear stress analysis and empirical fracture data, Moore provides a convenient tool for sizing glass for a given probability of failure due to uniform pressure loads such as wind and snow (20). For design purposes, a uniform loading of 50 lb/ft^2 is commonly used because it provides a low probability of being exceeded and has a minimal effect on module price (7).

Design and test techniques for hail-impact loading have also been developed in response to high levels of field failures with nonglass modules due to hail impact (7,21,22). Field experience indicates that resistance to 1-in.-diameter hail is required, even in low-hail-incidence regions of the country. This large size reflects the design margin required to achieve the low probabilities of failure outlined in Tables 1 and 2.

When amorphous-Si cells are deposited on the rear of the module superstrate, the high-temperature tin-oxide coating process anneals the glass and generally requires that the glass be either structurally backed up or retain some temper following the coating process. Large a-Si (30 x 30 cm) modules making use of 3 mm (0.125 inch) annealed glass have difficulty passing the JPL Block V hail test; however, both structurally supported and partially-tempered a-Si glass modules meet the requirement. The data indicate that glass strength is an important consideration with present-day thin-film modules and will become even more important as module sizes increase in the future.

Module open circuits

Module open-circuiting is the result of a major break in the module electrical circuit, generally involving the bus wiring or output connection. Although no quantitative statistical data have been gathered to this author's knowledge, such failures have been encountered at JPL with modest frequency during the failure analysis of field problems. Thermal differential expansion stresses and poor solder joints are the cause of many of the observed failures. It is expected that attention to these issues, together with careful qualification testing, will allow the levels in Tables 1 and 2 to be achieved.

Module hot-spot failures

A third cause of failures in both crystalline-Si and thin-film modules is excessive local cell hot-spot

heating that can occur when a cell or group of cells is subjected to a current level greater than the cell's short-circuit current. As shown in Figure 8, this condition can be caused by a variety of circuit faults such as cell cracking, local shadowing, and open-circuiting of series-parallel connections. When the degree of heating exceeds safe levels (100° to 120°C in most modules), the module's encapsulant system can suffer severe permanent damage (23,24). Preventing such damage requires the use of bypass diodes or other corrective measures to limit the maximum heating level. References 5, 23, 24 and 25 describe means of determining the number of bypass diodes required and test methods to verify that hot-spot heating is limited to safe levels. For most cell and module constructions, a bypass diode is required around every 10 to 15 series cells.

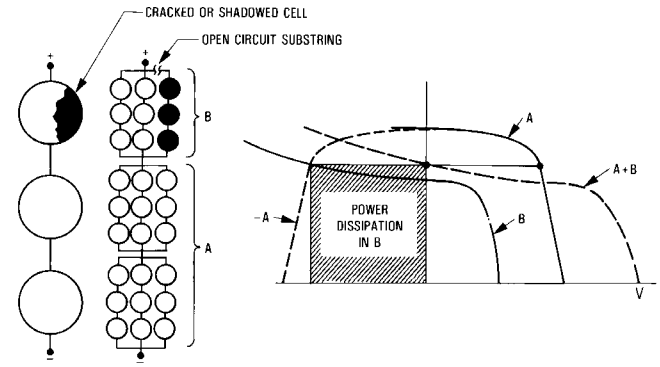


Figure 8. Visualization of hot-spot cell heating.

Failed bypass diodes

Although bypass diodes represent an important means of improving array reliability, at the same time they introduce additional failure mechanisms.

Like module open circuits, instances of internally shorted bypass diodes and diode shorts to ground have been observed, but not quantified. Recent work on diode reliability indicates that very little historical data are applicable to the PV module bypass application, which involves long periods of low (5-volt) reverse voltage together with periodic high forward currents. Because diode junction temperature is the critical factor related to long-term reliability, it is recommended that the junction temperature of silicon diodes be maintained below 125°C under conditions of maximum bypass current and ambient temperature. Detailed design requirements and test procedures are now available for bypass diodes (26).

Module shorts to ground

When modules are intended for use in high-voltage (>50 volt) applications, the cell circuit must be reliably isolated from the module frame and external surfaces. The general requirement is that the module leakage current from cell string to external surfaces must be less than 50 a when the applied voltage (cell to module exterior) is set to twice the worst-case system voltage plus 1000 volts. The maximum voltage stress includes consideration of maximum open-circuit array voltage achieved under low temperature (0°C) and high irradiance (100 mW/cm^2), as well as transient overvoltages due to, for example, system feedback of lightning transients. The latter is bounded by the characteristics of incorporated voltage-limiting devices such as MOVs. For most multi-killowatt-size applications, this (hi-pot) test voltage is in the range of 1500 to 3000 volts.

Meeting module voltage withstand requirements demands great care in the design of the module electrical insulation system for any module whether using crystalline-Si or amorphous-Si cells. Because voltage breakdown tends to occur at insulation flaws and sites of stress concentration, voltage withstand level is found to vary widely from module to module (27). Amorphous-Si modules using monolithically deposited cells on glass must additionally contend with the fact that the tin-oxide transparent conductor often causes the front surface and edges of the glass to be electrically connected to the cell string. This tin-oxide conductive path to the module exterior must be reliably interrupted and augmented with a high quality weather-resistant insulation system.

A second important requirement is the limiting of array leakage currents under normal operating conditions. This requirement is driven by the demands of array ground-fault detection systems, which require that normal leakage-current levels be below the threshold trip level set to note a voltage breakdown. The required leakage level is a function of the number of modules per detection system and the system operating voltage.

In addition to posing a safety hazard, module leakage currents also result in electrochemical corrosion of the solar cells. Electrochemical corrosion is caused by array leakage currents that lead to the migration of corrosion products between the solar cells and the module frame. With time, the products may bridge the insulation with a conductive path that results in a short to the grounded module frame. Mon, et al. (28,29) points out that the level of corrosion is proportional to the total integrated ionic leakage current (amp-hours) as influenced by module temperature and humidity conditions. Extensive research at JPL during the past 2 years has clarified the importance of this degradation mechanism and led to a much improved understanding of the governing design parameters (28,29).

Because ground-fault failures generally require immediate repair and often lead to plant shutdown, very low failure levels are required. For modules where breakdown is largely constrained to occur between the cell circuit and the module's peripheral frame, it is useful to address the allowable number of breakdowns per year per mile of module periphery. Tables 1 and 2 assume a linearly increasing rate of failures over the plant's life based on historical experience with voltage breakdown and the accrued damage characteristics of electrochemical corrosion. The indicated value of 0.01%/yr^2 corresponds to a failure rate of 0.1%/yr (or one

breakdown per 3 miles of module periphery per year) after 10 years.

Module delamination failures

Delamination of the module encapsulant system is another historical failure mode for terrestrial modules. It is heavily influenced by the choice of materials and processes. Although module designs of the mid-1970s often experienced high failure rates due to this mechanism, recent development of improved interface primers and laminating procedures has drastically reduced instances of early delamination in the field. Coulter, et al. (30) summarize the state of the art of module bonding technology and list effective interface primers for use in various module encapsulation systems. The art of life prediction or failure-rate prediction, however, is not well developed for the mechanisms associated with debonding. A significant contributing factor is the number and complexity of mechanisms involved. These involve processing sensitivities such as cleanliness and primer thickness, environmental reductions in bond strength due to moisture and photothermal aging effects, and increased module stresses due to material shrinkages and differential thermal and humidity expansion.

Tables 1 and 2 assume that we can eliminate the generic delamination encountered in the past, and reduce the problem to one of processing-induced random failures that increase over time due to environmental aging effects. Significant research is still required to relate where we are, quantitatively, to the economic requirements of Tables 1 and 2.

Life-limiting wear-out mechanisms

The last degradation category is the most difficult to quantify through known failure mechanisms. Most of the known mechanisms have been studied and found to be gradual or statistical in nature and not associated with a wear-out end of life such as might be associated with automobile tires or light bulbs.

Mechanical fatigue of cell interconnects is a classic example of a wear-out mechanism. However, to achieve the desired low rate of random interconnect failures during the early life of the array, the wear-out life associated with 10% failures will typically be more than 100 years.

Encapsulant failure due to depletion of UV absorbers and voltage breakdown due to electrochemical treeing are two mechanisms recently found to display life-limiting failure trends. With UV absorbers and other encapsulant stabilizers, there may be little degradation while the additives are slowly depleting over time. However, once the concentrations drop below critical levels, the encapsulant rapidly degrades.

Electrochemical-corrosion-induced voltage breakdown is similar to mechanical fatigue in that it is a mechanism associated with accrued damage. In this case, the relevant measure is total amp-hours of electrical charge transferred in the corrosion path.

With both mechanisms, it is not clear whether random failures due to processing variations or generic wear-out will govern. As a result, both mechanisms were also discussed above, under the category of module failures. From an end-of-life point of view, it is important that the annual cost of maintenance and replacement stay well below the annual worth of electricity produced until after 30 years.

Summary remarks

As part of the U.S. National Photovoltaic Program, the Jet Propulsion Laboratory Flat-Plate Solar Array Project has carried out a comprehensive array engineering activity addressed to understanding the reliability attributes of terrestrial flat-plate photovoltaic arrays and to deriving analysis and design tools useful for array optimization and cost reduction. Known array failure and degradation mechanisms have been carefully studied and grouped, for the purpose of discussion, into four categories. Target reliability allocations have been developed within each degradation category based on the life-cycle-cost requirements of future large-scale applications and the technical realities of available photovoltaic materials and processes. Comparison of these future requirements with present performance and design alternatives suggests that lives in excess of 30 years are very possible for the best available crystalline-Si module designs.

As an indication of the evolving nature and continuing growth of photovoltaic technology, thin-film amorphous-Si power modules have also made their commercial debut during the past 2 years. Although the reliability of these first-generation modules is not yet consistent with the needs of large-scale power applications, the technology is under vigorous development worldwide. Key research priorities include light-induced effects, cell corrosion leading to increased series resistance, glass breaking strength for large modules, and the development of protective encapsulants that meet the outdoor weathering and voltage isolation required for long-life modules.

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