

RESPONSE OF AMORPHOUS SILICON CELLS TO REVERSE BIASING*

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ABSTRACT

This paper discusses the results of a study to determine the hot-spot susceptibility of amorphous silicon cells and modules, and to provide guidelines and develop a qualification test for reducing module hot-spot susceptibility.

Amorphous cells are shown to have hot-spot susceptibility levels similar to crystalline-Si cells leading to the fact that the same general guidelines apply for protecting amorphous cells from hot-spot stressing as apply to crystalline-Si cells.

Recommendations are made on ways of reducing module hot-spot susceptibility including the traditional method of using bypass diodes and a method unique to thin-film cells, limiting the string current by limiting the cell areal size.

INTRODUCTION

Hot-spot heating occurs in a photovoltaic module when the short circuit current of a cell becomes lower than the string operating current causing the affected cell to go into reverse bias and absorb power equal to the product of the cell reverse-bias voltage and the string current. Field experience has demonstrated that hot-spot heating can lead to cell and module degradation.

Since the degree of hot-spot heating is a function of the series-parallel configuration of the circuit in which the cell is located, there are circuit-design techniques that can be used, both in a module and in an array, to ameliorate the effects of the heating. In the past, the primary technique for crystalline silicon modules was the use of bypass diodes which limit the reverse-bias voltage. A more important technique for amorphous-silicon modules is that of limiting current by limiting cell size.

In the past a laboratory test has been developed at JPL to determine the hot-spot susceptibility of crystalline-Si modules (1,2). The test conditions are meant to simulate the thermal boundary

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conditions for a 100 mW/cm^2 , 40°C ambient environment. This test, which has been used extensively in the qualification testing of modules, formed the basis for the testing described in this paper and the initial testing phase described in an earlier paper (3).

Initial testing was performed on three- and four-inch-square a-Si submodules, as well as, one-foot-square a-Si modules. These initial tests indicated that, because of the limited thermal capacity of thin-film cells, the amount of lateral thermal conduction provided by the substrates and superstrates has a significant impact on the hot-spot temperature incurred.

The principal objective of the current work was to develop guidelines that can be used by manufacturers of amorphous modules and arrays to reduce hot-spot susceptibility. A second key objective was to provide the PV community with a suitable hot-spot qualification test for amorphous-silicon modules.

APPROACH

The test procedures employed in the current task, modified as described previously (3), are essentially those used to test crystalline silicon cells (1,2).

The testing of modules with the cells sandwiched between two sheets of glass required that special test modules be prepared by the manufacturer. Several of the modules tested were of this type; for these modules a ribbon lead was attached along the back of each cell. This lead-attachment technique is also required to distribute the back-bias current along the entire cell surface area because of the poor conductivity of the transparent top conductor. Otherwise, with leads attached at the edge only, the hot-spots tend to occur at the same edge of the cell where the electrical leads are attached. This was the case with several of the other modules tested. Two current-input schemes were used with edge-attached leads. In one case, current was input at the same module edge to two adjacent cells. In the second case, current was input at opposite ends of the module for each of the cells. Figure 1 gives a schematic of the different current-input techniques used.

There are two kinds of cell reverse-quadrant characteristics that must be considered when selecting the hot-spot test parameters

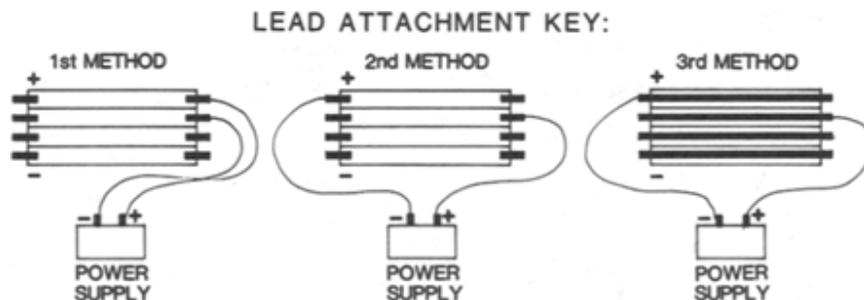


Figure 1. Schematic of the current-input techniques used.

of voltage, current, and illumination level. One kind, which manifests high shunt resistance (referred to previously as type A, (1,2,3)) exists when the back-bias voltage is limited only by the level of the applied voltage. The applied voltage is determined by the number of series cells per bypass diode, or the number of series cells in the array source circuit if no bypass diodes are used. This type of cell achieves the greatest amount of back-bias heating under conditions of partial shadowing.

The second kind of characteristic (type B) is associated with low shunt resistance cells where the breakdown voltage is less than the available back-bias voltage. Consequently, the hot-spot heating in these cells is limited by the available string current and the breakdown voltage of the cells, not the number of series cells as defined above. The back-bias voltage of these cells reaches its maximum value under conditions of full shadow; therefore, low-shunt-resistance cells suffer the greatest hot-spot heating dissipation when fully shadowed.

In the experiment conducted the back-bias current and voltage were provided by a power supply; a chart recorder was used to record the reverse-quadrant response of the test cell. A radiant heating source was used to raise the test-cell temperature to the nominal operating cell temperature (NOCT). The hot-spot temperature was measured with an infrared (IR) camera. This method provides a parametric representation of power dissipation versus hot-spot temperature for the test with recording of the hot-spot temperature as the test proceeds. A photograph of the test setup is shown in Figure 2.

Both exploratory testing and the standard 100-hour cyclic hot-spot susceptibility test were performed on cells in several modules. The tests simulated operation at short circuit and at a field operating temperature of 45-50°C. The cells were found to be type B cells and the tests were performed in the absence of illumination as discussed below.

Actual hot-spot-test acceptance criteria (2) involve a visual

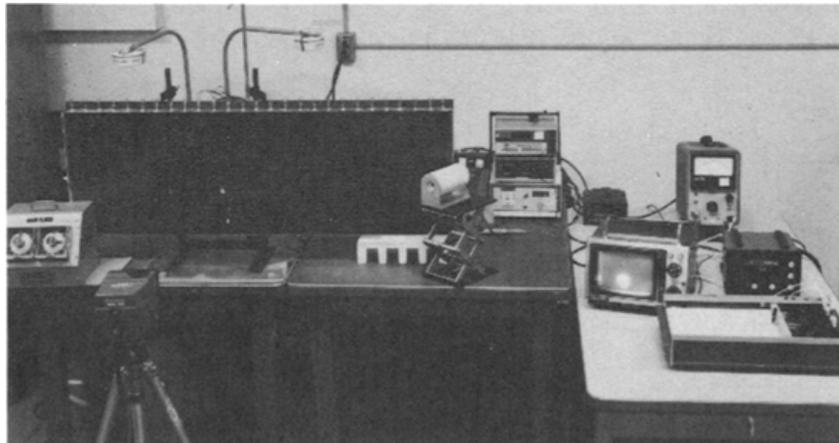


Figure 2. Photograph of hot-spot test setup.

inspection, a post-test electrical performance measurement, and an isolation test. The study discussed here did not involve the latter two tests.

OBSERVATIONS AND RESULTS

The overall response of amorphous-silicon cells to back biasing is similar to crystalline cells with several notable exceptions. The most significant difference between the second-quadrant responses of amorphous and crystalline cells is the lower and more sharply defined breakdown voltage in the current-voltage curve of amorphous cells. The most important consequence is that a cell in series with more than 10-15 cells will act as a type B cell with the back-bias voltage limited by the breakdown voltage. Therefore, hot-spot tests performed on modules with more than this number of cells should be performed in the absence of illumination, as were the tests performed on the modules in this study.

In general, amorphous cells are more sensitive to back-bias conditions than crystalline cells, exhibiting rapidly changing characteristics, some more so than others. As discussed previously (3), amorphous cells exhibit a dichotomous behavior in their second quadrant response with initial back biasing indicating a high shunt resistance with a sharp voltage breakdown in the 8-12 volt range. After thermal runaway and subsequent cool down the cells have a lower shunt resistance. Figure 3 compares some typical second-quadrant responses of the cells from three different manufacturers that were tested.

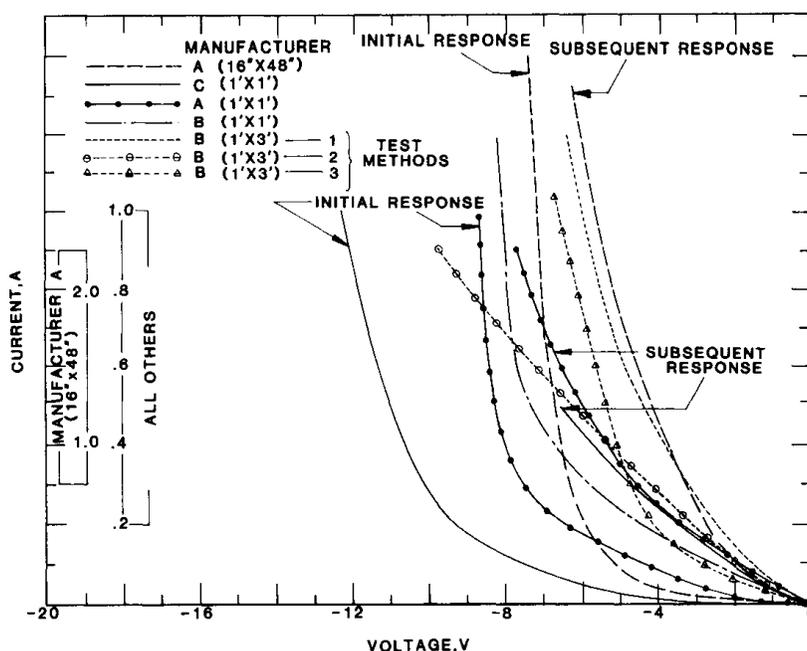


Figure 3. Typical amorphous-cell-second-quadrant I-V curves.

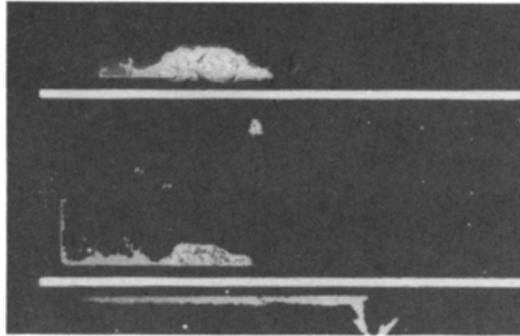


Figure 4. Photograph of hot-spot-induced cell erosion.

Another interesting phenomenon was the occurrence of multiple hot-spots where there is a shift of the dominant hot-spot (one with highest temperature) among the different hot-spots. In some cases this resulted in the sharing of power leading to lower hot-spot temperatures for the same total power dissipated. The visual effects observed were cell erosion, cracked glass, encapsulation discoloration, blistering of the module backing, and arcing. Except for cell erosion, not all of the effects were noted on all modules. For instance, cracked glass was most prevalent on modules with only one layer of glass. Cell erosion refers to the apparent highly localized loss of cell material from the hot-spot area, and is shown in Figure 4, which is a photograph of one of the cells tested. Cell erosion has two effects on the cell performance. It can lead simply to loss of power resulting from the loss of cell area, or, in addition, it can lead to increased shunting of the cell.

As explained previously (3), a direct dependence does not exist between the highest temperature achieved on a cell and the total power dissipated in the cell. However, it is useful to bound the range of observed temperatures for a given power dissipation because the temperature obtained can be related to the effects observed in cells and module materials.

Experience with crystalline-silicon cells (1) indicated that the onset of degradation occurs in the 120-140°C range, with severe degradation occurring above that range. In the case of amorphous cells, erosion started at about 80°C and became quite noticeable above 120°C. In one module cracked glass was noted even at the relatively low temperature of 100°C. As with crystalline cells, most of the effects were noted above 120°C.

Figure 5 gives a plot of the temperature rise above NOCT per hot-spot power dissipated for the modules of three manufacturers; the cells and modules were of various sizes as noted. The spread in data for the same module type is indicative of the variable dependence of temperature on power dissipation. The variability in the observed data also is a function of the differences in the heat-sinking capability of the modules. This latter aspect was made evident when glass cracking occurred in modules with a glass superstrate and no

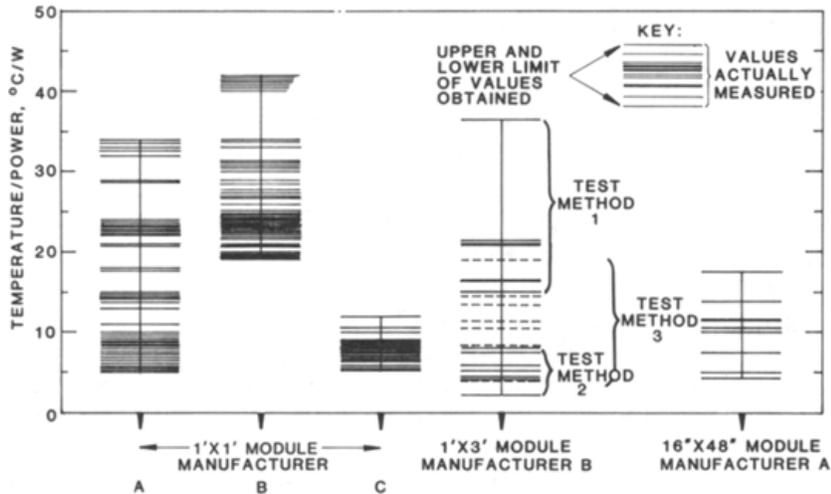


Figure 5. Temperature rise above NOCT per watt of hot-spot power dissipation.

substrate, and not in modules with a combined glass super/substrate twice as thick.

RECOMMENDATIONS AND CONCLUSIONS

Figure 6 gives the hot-spot temperature as a function of back-bias current for some of the modules tested. This type of plot is particularly significant for amorphous modules. For crystalline-silicon modules the best technique to ameliorate hot-spot heating is the use of bypass diodes, which limit the potential back-bias voltage. However, the use of bypass diodes with amorphous modules is less advantageous for two reasons. First, since they tend to have higher voltages for the same size as compared to crystalline

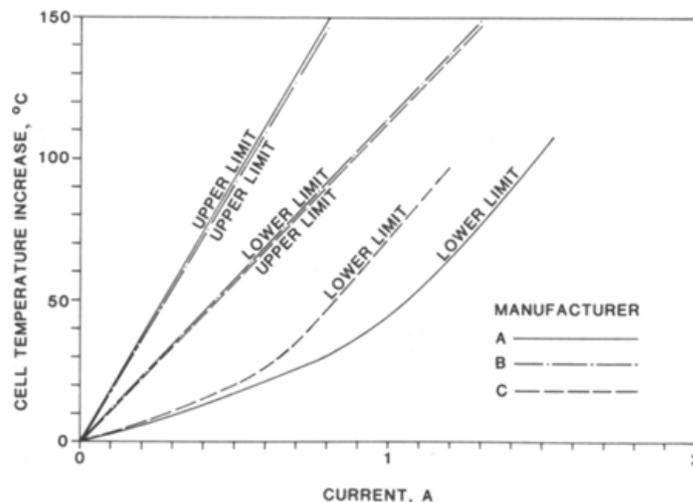


Figure 6. Hot-spot temperature as a function of back-bias current.

modules, and the cells have lower breakdown voltages, multiple diodes would be required internal to each module. Secondly, bypass diodes are difficult to integrate easily into the monolithic structure of a-Si module circuits. Because hot-spot heating can also be controlled by reducing the available current, a promising approach to controlling hot-spots in an a-Si modules consists of limiting the cell size (and thus the current) by scribing a module into two or more parallel strings of smaller cells. Plots such as Figure 6 are useful as guidelines for determining maximum cell size to limit hot-spot temperature to a given level.

A second approach for reducing hot-spot temperature involves improving lateral heat transfer within the module. The actual hot-spot temperature reached is a strong function of the amount of lateral thermal conductance provided by the module's glass superstrate and substrate. Thus, the thermal design of the module can be used to ameliorate hot-spot heating and reduce the module's susceptibility to back biasing. This is illustrated in Figure 5 where the hot-spot temperatures of modules with different lateral thermal conductances are compared.

The use of bypass diodes with amorphous cells to reduce back-bias voltage requires consideration of the low cell-breakdown voltage. If diodes are required it means that the voltage must be reduced below 8-12 volts and therefore the diode frequency must be at least one diode every 10-15 cells. This implies that the diodes must be mounted internally in modules having more than this many series cells. The use of diodes should be traded off against reducing cell size to lower the current, and also against improved lateral heat transfer to reduce the hot-spot temperature.

HOT-SPOT QUALIFICATION TEST FOR AMORPHOUS SILICON MODULES

The recommended hot-spot qualification test for amorphous silicon modules (1,2) is basically the same as for crystalline silicon modules. One unique consideration for a-Si modules is the difficulty in attaching electrical leads to the individual cells within a module. The leads are required to carry full one-sun ($100\text{mW}/\text{cm}^2$) current and must distribute the current into the cells without causing excessive current crowding near the lead attachment or shunting of the cell by damaging the thin cell metallization. Another important consideration is minimizing disturbance of the cell's poor lateral electrical conductance which resists the ability of the module current to crowd into a highly localized hot spot. Attaching leads along the entire length of the cells reduces the current crowding near the attachment point, but increases the chance of cell shunting and greatly reduces the natural resistance to current crowding into a hot-spot region.

An alternative lead-attachment approach is to attach to opposite ends of the adjacent cells. This requires that the current flow down the entire length of the cells, thus introducing the natural sheet-resistivity in series with the hot-spot shunt. However, current crowding near the lead attachment is a possible problem.

None of these lead-attachment techniques as used was completely without problems. More testing and comparison of the results obtained using different attachment techniques is required before a final recommendation can be made.

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