Design Guidelines for Large Photovoltaic Arrays

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The BDM Corporation

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FOREWORD

This report, BDM/TAC-78-686-TR, is submitted by The BDM Corporation, 2600 Yale Blvd. S.E., Albuquerque, New Mexico 87106, to Sandia Laboratories, Albuquerque, New Mexico 87115. This report is in fulfillment of Task 3 of contract 07-6941, and presents guidelines for electrical design of photovoltaic modules and arrays for large scale applications. The program is under the direction of M. G. Semmens. The principal contributors to Task 3 were R. M. Turfler, T. J. Lambarski and R. W. Grant.
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CHAPTER I
INTRODUCTION

A. OVERVIEW

1. Objectives

The purpose of this document is to provide system design engineers with guidelines for protecting cells and obtaining optimum performance in the design of large photovoltaic arrays in normal and adverse illumination environments. Three environments are considered here: uniform illumination, selective shadowing, and illumination transients such as lightning.

Only electrical considerations are addressed in these guidelines. Economic, mechanical, civil, etc., factors are not within the scope of this contract. However, these factors are discussed briefly in Chapter II, Initial Design, and costing impacts are identified qualitatively in the protection and performance guidelines where appropriate.

The guidelines are keyed toward system design engineers who have a working knowledge of both electrical and mechanical design concepts. The guidelines provide a basic understanding of the design considerations and simple methods for estimating design tradeoffs in general cases. These methods can be applied to specific cases without computer simulation. For more exact answers to detailed questions, more complex analyses, possibly supported by computer simulation such as PV-TAP (the Photovoltaic Transient Analysis Program) (described below) may be required.

2. Background

These guidelines are presented as the final product of a contract sponsored by DOE and Sandia Laboratories to provide tools for designers and analysts of large photovoltaic arrays. Earlier phases were devoted to development of a computer code for analyzing nonlinear electrical and thermal response of photovoltaic system elements to electrical and illumination transients. PV-TAP, which resulted from this effort, is a major update of NET-2, a general purpose, nonlinear
network analysis code capable of handling a wide variety of electronic network components as well as problems arising in other engineering fields. In addition to all the capabilities of NET-2, the PV-TAP code also includes photovoltaic cells, aggregation of cells, collectors, heat transfer networks, and other PV system elements.

3. Format

Introductory and background material are presented in this chapter. The design guidelines are presented in subsequent chapters, following the three major steps employed in designing an array. The first step in designing an array is the initial design, in which design requirements, power conditioning, cell and collector selection and the basic wiring pattern are determined. The next step is design of the basic module and protection against burnout. Finally, the array is "built up" by interconnecting modules to obtain the desired power requirements in the most efficient configuration. Hand calculation techniques have been employed wherever possible, supplanted by PV-TAP runs when needed.

B. BASIC CELL OPERATION

In order to use the guidelines presented in this report, a basic understanding of photovoltaic cell operation is required. The following section details the operation of the Ebers-Moll model used in this report. Symbols and terminology will be the same throughout the report.

The photovoltaic cell is basically a PN junction diode. The behavior of the cell can be modeled with the Ebers-Moll circuit analog model shown in figure 1-1. The current source, $I_D$, is given by the normal PN junction diode equation,

$$I_D = I_{ST} (e^{V_D} - 1)$$

where $I_{ST}$ = saturation current at a given temperature

$\theta$ = emission constant

$V_D$ = junction voltage.
Figure I-1. PV Cell Model

$I_P$ = LIGHT-GENERATED PHOTOCURRENT

$I_D$ = STANDARD DIODE JUNCTION CURRENT

$C_J$ = JUNCTION CAPACITANCE

$R_{SH}$ = SHUNT RESISTANCE

$R_S$ = SERIES RESISTANCE
The current source, $I_p$, is the photocurrent generated in the junction. It can be approximated by the short circuit current, $I_{SC}$, measured at a given insolation and temperature. The photocurrent increases linearly with insolation but varies only slightly with temperature over the normal operating ranges. $C_J$ is the junction capacitance. The shunt resistance, $R_{SH}$, determines the amount of current leakage across the junction due to ohmic defects. The series resistance, $R_S$, is a combination of the bulk resistance and resistance due to contacts.

The PV cell is operated with no external bias. When illuminated, a photocurrent, $I_p$, is produced across the junction as indicated in figure I-1. This will produce a current in the external load with the positive direction as indicated. If the anode is shorted to the cathode, essentially all the current will flow through the external terminals and the output voltage will be zero. This condition is represented by the short circuit current, $I_{SC}$, in the typical I-V curve shown in figure I-2. The basic shape of the curve is determined by the diode current, $I_D$, which is exponential. When a discrete load is placed across the terminals, the voltage developed across this load biases the junction, causing some of the photocurrent to be shunted through the junction. This current, consisting mostly of $I_D$, subtracts from the photocurrent, reducing the current available at the output.

At the other extreme is the open circuit voltage, $V_{OC}$, which is obtained when the terminals are disconnected. $V_{OC}$ is determined by the diode equation since essentially all of the photocurrent passes through and forward biases the junction. $V_{OC}$ increases logarithmically with insolation since it is determined by the photocurrent, $I_p$, being forced through the junction as $I_D$. Conversely, $V_{OC}$ decreases with temperature since the saturation current, $I_S$, in the diode equation increases with temperature. This means that the junction is unable to sustain the same voltage at higher temperatures.

The shape of the curve in figure I-2 is also dependent on the values of $R_{SH}$ and $R_S$. These resistances cause the curve to deviate further from a rectangular shape. Small values of $R_{SH}$ will shunt some
Figure I-2. PV Cell I-V Curves
of the photocurrent, reducing the current available at the output at all values of voltage. At open circuit, the current in the shunt resistor will reduce the current available to the diode equation, reducing \( V_{OC} \). Large values of series resistance will reduce the output voltage at all values of current. In short circuit conditions, the current through the series resistance will cause a voltage at the junction which will shunt some current through the junction elements, \( I_D \) and \( R_{SH} \). This will cause \( I_{SC} \) to be lower than the photocurrent, \( I_P \).

The normal output from the cell described by figure I-2 would be about 1.3 amperes at 0.45 volts. Higher voltages and currents can be obtained by placing cells in series and parallel. When identical cells are placed in series, as in figure I-3(a), the current of the string is the same as that from one cell but the voltage is the sum of the individual cell voltages. Thus, for four cells in series, the current is still 1.3 amperes, but the voltage is \( 4 \times 0.45 = 1.8 \) volts.

When identical cells are connected in parallel as in figure I-3(b), the voltage of the string is the same as that from one cell, but the current is the sum of the individual cell currents. Thus, for four cells in parallel, the voltage is 0.45 volts, but the current is \( 4 \times 1.3 = 5.2 \) amperes.

C. ILLUMINATION ENVIRONMENTS

Three types of illumination are considered in this report, 1) uniform steady state, 2) nonuniform steady state, and 3) uniform transient illumination.

Uniform steady state illumination simulates normal cloudless sunlight which varies over the course of the day, but the variation is slow compared to the response time of the PV cells. Nonuniform steady state illumination represents shadowing of parts of the array by slow-moving clouds and stationary objects. Another slow illumination transient which is unique to linear parabolic trough concentrators is shadowing of cells at the end of a collector when the sun is low in the sky.
V = 1.8 V  
I = 1.3 A  
(a) SERIES CONNECTED CELLS

V = 0.45 V  
I = 5.2 A  
(b) PARALLEL CONNECTED CELLS

Figure I-3. Series-Parallel Trade-offs
effects). These are considered steady state because the variations are slow compared to the response time of the PV cells.

Transient illumination consists of lightning outdoors or high-speed electronic flash simulations in a laboratory.

These illuminations can cause reverse bias and/or heating which can burn out the cells and break the connections. Shadowing and lightning can also reduce performance efficiency. These effects will be discussed in chapters III and IV.

D. DESIGN PROCEDURE

Figure I-4 illustrates a typical procedure for designing a large photovoltaic array. In the Initial Design phase, the desired power level and terminal conditions are specified. The power conditioning and load matching philosophies are chosen. Cell and collector types are chosen. An initial series-parallel wiring pattern is selected and integrated with the collector/cell types to determine an initial collector mounting configuration and collector arrangement.

Next, the basic module composed of individual cells interconnected in some basic series-parallel scheme and mounted in a package is designed and protected against burnout by the proper placement of blocking and bypass diodes.

Finally, the performance of the array is optimized by evaluating its response to various illumination conditions and making design changes as needed. The entire process is iterative. At each step, the initial design may be updated based on the results of the module protection analysis and/or array performance optimization. Each time the basic design is changed, it should be re-evaluated for burnout protection before being accepted.

Figure I-4 is an outline of the process. In subsequent chapters, each phase is broken down and illustrated in detail.
Figure I-4. Design Process Block Diagram (Overview)
CHAPTER II
INITIAL DESIGN

In this chapter a typical system design process is outlined and discussed. Design constraints which influence the results and the interdependence of the various aspects of the process are also discussed. Only basic considerations of system design are addressed since the contract covers only the electrical response of PV cells and arrays.

The bibliography contains numerous documents discussing photovoltaic system design trade-offs. The designer is urged to keep abreast of the efforts in progress in the various Department of Energy "Photovoltaic Experiments" contracts awarded under the PRDA's listed in the bibliography.

A. DESIGN PROCESS

A typical Initial Design process is illustrated in figure II-1. The process begins with an analysis of the design constraints. After these are fully specified and understood, two parallel efforts are initiated. An Economic Analysis gathers data on system components and technologies which satisfy the applicable design constraints. At the same time, generic system types which satisfy applicable design constraints are analyzed with preliminary inputs from the market survey. The results of the parallel studies are then used to reduce the number of candidate hardware combinations. These candidates are analyzed in detail before the most promising hardware are selected for the system. Finally, a series/parallel cell pattern is formulated for refinement in phases II and III of the overall design process.

The initial design phase is a complicated process and may require many iterations because of the interdependence of the results. In addition, the design may require revision based on results of phases II and III of the design process.
Figure II-1. Design Flow for Initial Design Process
B. DESIGN CONSTRAINTS

Design constraints are the key to setting up analyses and making hardware decisions. In many cases, one or more design constraints will provide clear direction and reduce the scope of the economic analysis and system analysis. Therefore, the design constraints should be clearly defined and carefully evaluated. They should also be continually referenced as criteria throughout the design process to assure applicability of the analyses being conducted and the hardware candidates being considered. Typical design constraints are listed in figure II-2. These apply to any system being designed but will be modified, expanded and personalized for the specific application under consideration. Some typical questions inherent in the design constraints include:

1. Will the system output be AC or DC?
2. How much ripple or distortion will the load tolerate?
3. Will the thermal energy generated be used?
4. How much of the electrical or thermal load profile can be economically matched with the available area?
5. Is a utility interface available at the location?
6. Are there unavoidable shadow sources?
7. Will the system be actively cooled?
8. Will the collectors be flat plate or concentrating?
9. Will the collectors be fixed or tracking?
10. Does the statement of work specify a type of system or specific design feature?

C. INITIAL PARALLEL STUDIES

1. Economic Analysis
   The economic analysis provides a data base for the systems analysis and the hardware definition activities. Data are gathered on cost, availability and performance of power conditioning equipment, collectors, PV cells, cooling systems, monitoring equipment and other
DESIGN CONSTRAINTS

ELECTRICAL LOAD CHARACTERISTICS
- TYPE AND QUALITY
- LOAD PROFILE

THERMAL LOAD CHARACTERISTICS
- TYPE AND QUALITY (TEMPERATURE)
- LOAD PROFILE

GEOPHYSICAL TOPOGRAPHIC DATA
- LOCATION
- AVAILABLE AREA
- TERRAIN

ECONOMIC CONSTRAINTS
- DESIGN FUNDS AVAILABLE
- TARGET OPERATING COSTS

MISCELLANEOUS CONSTRAINTS
- CONTRACTUAL
- LEGAL
- AESTHETIC

SYSTEMS ANALYSIS

ECONOMIC ANALYSIS

HARDWARE DEFINITION

PHASES II AND III

Figure II-2. Enumeration of Design Constraints
related equipment which meet the design constraints previously established. Data should include expected lifetime, reliability, maintenance requirements and cost, operating specifications, size, weight, safety features and many more. Current data and conservative projections for improvements by the procurement date should be included. Only preliminary rough cut data and data of a generic nature are required for the system analysis while data for hardware analyses should be as complete as possible. (See figure II-3.)

2. System Analysis

Based on the design constraints previously established, analyses are performed on generic systems. The analyses are designed to answer many of the questions listed above in the section on design constraints. Thus, specific hardware is not analyzed but rather general issues concerning the desirability of such features as battery storage, power tracking, concentrating collectors, active cooling, utility interface and various cell technologies are addressed.

The analyses can be performed using hand techniques and computer simulation. Programs such as SOLCEL are very useful for this type of analysis. SOLCEL is a simulation program designed specifically for photovoltaic systems analysis and design optimization. Photovoltaic conversion modeling is based upon cell parameters. Concentrating, non-concentrating, tracking and nontracking systems are available for simulation. Other subsystem models included are power conditioning, energy storage, and either utility or diesel generator backup. Total subsystem performance may be evaluated using either life cycle or levelized busbar energy costing methods. A self-contained routine allows the system performance to be optimized relative to subsystem or component sizing for a defined load and insolation data base. The program is available from Sandia Laboratories, Albuquerque, Photovoltaic Systems Definition Project Division.

The generic studies are interdependent and iterative in that the results of various analyses may provide requirements for additional generic analyses or may force repetition of previous analyses with revised inputs.
Figure II-3. Details of Initial Parallel Studies
D. HARDWARE DEFINITION

The design process for hardware definition is illustrated in figure II-4. Based on the market survey and the generic studies, the answers to such alternatives as active versus passive cooling and flat plate versus concentrator lead to a reduction of the candidate hardware combinations under consideration. The candidate hardware combinations are analyzed with specific hardware data using hand techniques and computer simulation such as SOLCEL. Analyses are reiterated as needed to eliminate candidates whose performance is not cost-effective. Details such as collector sizing and orientation, power conditioning and energy storage design, and coolant velocity and temperature are considered.

Based on these analyses, the most promising hardware combination is chosen and analyzed to determine the optimum design parameters. Hardware selection or preliminary design options may require updating and re-analysis. The degree of reiteration will depend on the complexity of the system and the clarity with which the design constraints are understood. Therefore, the design constraints should be continually reviewed and updated if needed.

As one of the results of these analyses, terminal conditions are specified. The voltage-current ratio determines the ratio of series to parallel connections. The cells are arranged within the collectors in a preliminary series-parallel pattern which may be revised based on results of phase II and III, Module Protection and Array Performance Optimization. The preliminary series-parallel pattern selected may affect collector and cell design conditions and specifications such as shadow patterns, collector length and cell dimensions. These may in turn require some redesign of the prototype system.

It should be remembered throughout that many of the design steps are interdependent and changes in one design feature may produce changes in others.
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Figure II-4. Details of Hardware Definition

II-8
Once the initial design has been specified, the next step is to design the basic module. Figure III-1 shows the Design Flow for module design. The applicable initial design results are shown as inputs to the process. The most important design consideration is prevention of failures due to electrical overstress (burnout) and overheating (thermomechanical failure). Electrical overstress is limited by careful placement of bypass diodes to prevent cells from experiencing high reverse bias and breakdown. In a long series string, some cells can be forced into reverse bias if they have photocurrents which are significantly lower than the average or if they are shadowed. The degree of reverse bias is dependent to a large extent on the number of cells in series. The addition of bypass diodes breaks up a series string into smaller series strings reducing the maximum reverse bias attainable across any individual cell. This is discussed in more detail in subsequent sections.

The temperature rise is presented as a function of cell operating conditions and illumination conditions. To permit a general solution, the rise is given relative to the temperature rise for a cell operating at open circuit under full design illumination. It is assumed that the designer will consider the temperature rise of an open circuit cell at full design illumination as part of the initial design.

Cost impacts are not discussed in these guidelines. However, the cost of implementing any design improvements should always be considered and alternate methods of accomplishing the objections more economically without sacrificing cell protection should be evaluated.

A. FAILURE MECHANISMS

All of the failure mechanisms associated with the photovoltaic cell are basically the result of overheating some portion of the cell, such as solder joints, metalization strips on the illuminated surface, or the PN
Figure III-1. Design Flow for Module Protection
junction. Figure III-2 shows the heat flow in a PV cell from the edge view. The arrows into the upper surface represent the power deposited by the sunlight. The electrical contacts shown at the left edge may either remove power as in the normal operating mode, or deposit power as in reverse bias operation. Under normal operating conditions, the insolation power is uniformly deposited across the cell and the electrical power is relatively uniformly removed from the cell. The remaining heat must be dissipated through the substrate to the heat sink as indicated by the arrows below the cell.

By contrast, however, the electrical power deposited when the cell is operating in reverse bias can under some circumstances be deposited in a small volume due to defects in the cell. Under these conditions of localized heating, the effective thermal resistance is greatly increased due to the small area dissipating the heat. Under normal conditions where the heat is uniformly deposited, the effective thermal resistance may be calculated from the cell geometry. In reverse bias when localized heating is taking place, the effective thermal resistance cannot be accurately modeled, since it is dependent on geometric parameters which cannot be practically determined. Therefore, two failure mechanisms will be considered: overheating due to uniform energy deposition, and reverse bias overvoltage. Failure due to reverse bias overvoltage is said to have occurred when the reverse bias voltage is sufficient to cause non-uniform heating and failure in some devices. The problem of uniform overheating was analyzed at the individual cell level and is discussed in section D. Reverse bias overvoltage is controlled by the module design and is discussed in sections B and C.

The thermal transient due to the lightning illumination pulse is included in the cell analysis and discussed in section D. The effect of the lightning illumination transient on the worst case reverse bias cell voltage is discussed in section C.
Figure III-2. Heat Flow in a Photovoltaic Cell

* POWER REMOVED = V x I
B. ARRAY CONDITIONS CAUSING REVERSE BIAS CELL

The purpose of the array analysis is to demonstrate the system response to transients and to illustrate how nonuniform transients (or short circuit current tolerance) can cause individual bypass groups or cells to go into reverse bias operation. To illustrate how nonuniform illumination (or short circuit current tolerance) can cause reverse bias, consider figure III-3 which shows one string driving a load. Since all the cells in the string are in series, the same current must flow in each cell. Under normal operating conditions and full design illumination, typical array operating voltages are in the range of 200 to 450 volts. The ratio of peak power cell voltage ($V_{ppc}$) to open circuit cell voltage ($V_{occ}$) is typically in the range of 0.75 to 0.85 for single crystal silicon cells at design insolation. Therefore, the open circuit string voltage ($V_{ocs}$) is typically in the range of 235 to 600 volts. However, the current flowing through the string reduces the operating voltage of each cell from the open circuit cell voltage such that the operating voltage of the string is equal to the voltage of the load. If one cell is completely shadowed so that it produces no current, then there can be no current flowing through any of the other cells (assuming the shadowed cell does not go into reverse breakdown and fail and neglecting the shunt resistance of the shadowed cell). Therefore, all the illuminated cells in the string are operating at their open circuit voltage which is $V_{ocs} - V_{occ}$ or 234.3 to 599.5 volts. However, the voltages around the loop must add up to zero; that is, 234.3 to 599.5 volts for the illuminated cells minus 200 to 450 volts for the load must equal the reverse bias voltage of the shadowed cell. Therefore, the shadowed cell would have 34.3 to 149.5 volts reverse bias, which is well above the maximum safe reverse voltage of most cells and can be expected to cause failure. If the shadowed cell is not completely dark, it will produce some current and the operating conditions of the string will be somewhere between uniform illumination and complete shadowing of one cell. That is to say, the shadowed cell will be operating somewhere between the normal operating voltage of +0.38 to 0.6 volts and reverse voltage of 34.3 to 149.5 volts.
Figure III-3. One String Driving the Load with One Cell Shadowed
The maximum reverse bias voltage which can appear across any individual cell is limited by placing bypass diodes around each bypass group as shown in figure III-4. In exactly the same manner as in the string, the shadowed cell blocks current flow through the remaining cells in the bypass group. Therefore, the illuminated cells are operating at their open circuit voltage. Again, the voltages around the loop must sum to zero. For a bypass group composed of eight cells operating at the design temperature and full design illumination, the seven illuminated cells will produce approximately 3.5 to 4.9 volts. Assuming that the bypass group is reverse biased and the bypass diode is conducting the current generated by the remaining bypass groups, the voltage across the bypass diode will be typically between 0.6 and 1.5 volts. This will limit the reverse bias voltage across the shadowed cell to between 4.1 and 6.4 volts.

C. REVERSE VOLTAGE PROTECTION

The purpose of this analysis is to demonstrate the effect of shadowing and lightning illumination transients on cell operating voltage, and to provide guidelines for limiting reverse cell voltage to safe operating levels. As discussed in the preceding section, nonuniform illumination can cause reverse bias cell operation, and bypass diode placement must be chosen to limit the reverse bias voltage to within the safe operating limits. The following sections will first provide an example illustrating cell operating voltage under various shadowing conditions and module operating conditions. Then the relationship between the maximum number of cells in a bypass group and the maximum safe reverse bias operating voltage for one cell is explained under worst case module operating and illumination conditions.

In this example, a bypass group composed of eight cells is operated from short circuit through open circuit load conditions with seven cells operating at full illumination and one cell operating at illumination between zero and full design illumination. The module is loaded with a
Figure III-4. One Module in Reverse Bias with One Cell Shadowed
resistor whose value is varied to simulate various load conditions from open circuit through short circuit. The current from the bypass group is shown on the vertical axis, the voltage of the bypass group on the horizontal axis in figure III-5 with a single cell operating at 0, 25, 50, 75, and 100 percent of full design illumination represented by X, 1, 2, 3, and 4, respectively. This figure illustrates how shadowing one cell limits the current from the whole string. As previously discussed, shadowing one cell limits the current output of the string and can result in reverse bias of the shadowed cell. The operating voltage of the shadowed cell is shown on the vertical axis and the voltage of the bypass group on the horizontal axis in figure III-6. Figure III-6 represents the same conditions as figure III-5; that is, they have the same horizontal axis and the shadowed cell is operating at the same five illumination levels with the same plotting symbol representation. When all cells are fully illuminated, as represented by the 4, the cell voltage is always positive. However, when the shadowed cell is operating at 75 percent of design illumination, as represented by the 3, it goes into reverse bias when the module voltage drops from the open circuit level of about 4.8 volts down to approximately 3.5 volts. Note that as the shadowed cell is more completely shadowed, it goes into reverse bias for module operating voltages which are closer to the open circuit module voltage and it is driven farther into reverse bias when the module is operating at short circuit. Further, when the shadowed cell is completely shadowed, no current is produced and the shadowed cell remains in reverse bias for any resistive load on the module. Figure III-6 clearly shows that the worst case reverse bias is produced by completely shadowing one cell while the remaining cells remain at full illumination and the module is operated in reverse bias.

As discussed in section III-8 and illustrated in figure III-4, when one cell in the string is fully shadowed it produces no current and the remaining cells operate at their full open-circuit voltage. If the bypass group is reverse biased as shown in figure III-4, the voltages around the loop must sum to zero as shown below.
Figure III-5. Current Through Bypass Group vs. Voltage Across Bypass Group
Figure III-6. Voltage Across Shadowed Cell vs. Voltage Across Bypass Group
The maximum safe reverse cell voltage will be different for different types of cells (Si, GaAs, etc.), different concentration ratio and different cell manufacturers. Concentrator cells generally have a lower safe reverse voltage than flat plate cells. One cell manufacturer recommends that some presently available concentrator cells be subjected to no more than 5 volts reverse bias. The maximum safe reverse cell voltage must be obtained for the particular cell being used.

The relationship between the number of series cells per bypass diode and the safe reverse cell voltage is illustrated in figure III-7 for two values of the bypass diode forward voltage and two values of the open-circuit voltage. The forward voltage on the bypass diode depends on the size and type of bypass diode, but the range of forward voltages can be expected to fall between 0.6 and 1.5 volts for most diodes. The open circuit cell voltage \( V_{OCC} \) of 0.585 volt is typical of the open circuit voltage at full design illumination while 0.83 volt is typical of the open circuit voltage for the same cell due to a lightning illumination transient of 100 suns. As discussed in the following paragraph the worst case bypass group operating conditions coupled with a significant increase in open circuit voltage due to high intensity lightning illumination represents a very unlikely combination. A conservative design approach is to use the open circuit cell voltage plus some percentage (suggest 10 to 20 percent) as a safety factor.

Heating due to lightning is discussed in detail in section III-D. It will be shown here that lightning can produce no worse reverse bias than already considered due to shadowing, and therefore, need not be analyzed for reverse bias failure. If lightning is to produce more
<table>
<thead>
<tr>
<th>$V_f (V)$</th>
<th>$V_{oc} (V)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>0.6</td>
</tr>
<tr>
<td>2</td>
<td>1.5</td>
</tr>
<tr>
<td>3</td>
<td>0.6</td>
</tr>
<tr>
<td>4</td>
<td>1.5</td>
</tr>
</tbody>
</table>

Figure III-7. Number of Series Cells per Bypass Diode Versus Safe Reverse Cell Voltage
reverse bias on a cell than normal shadowing transients, worst case conditions must be maintained. Thus, one of the cells must be completely shadowed while the remaining cells being bypassed are completely illuminated and the bypass group is reverse biased. The probability of one cell being completely shadowed while the other cells in the bypass group are fully illuminated by a lightning flash is dependent on the geometry of the array. However, the probability is quite low that part of a bypass group would be brightly illuminated while the bypass group as a whole is reverse biased.

There are two major reasons for this important difference between normal illumination and lightning illumination. First, the normal illumination is approximately uniform across the array while high intensity lightning illumination would result from a very near strike. A near strike would be different distances from different parts of the array. This range of photocurrents reduces the combined open circuit voltage of the array. As the previous analysis showed, the difference between the open circuit array voltage and load voltage can cause reverse bias of a bypass group only when the current produced by the bypass group is below the current flowing in the rest of the string. Thus, the areas of the array with low insolation will limit the current produced by the string, thereby reducing the probability of reverse biasing a bypass group in the highly illuminated section.

The second and perhaps more important difference between normal and lightning illumination is caused by the series resistance. At illumination levels many times the design levels, the series resistance limits the output current. The current limiting effect is illustrated in figure III-8 with a simplified photovoltaic cell model. Under normal illumination the voltage drop across the series resistance \( R_S \) is small and the output voltage \( V_{OUT} \) is approximately equal to the junction voltage \( V_J \). However, high intensity lightning illumination produces so much photocurrent \( I_P \) that even under short circuit conditions \( V_{OUT} = 0 \), the voltage drop across the series resistance is near the open circuit cell voltage. However, the photocurrent is much larger than the short circuit.
\[ I_p = I_{p0} S \]
\[ I_D = I_{ST} e^{V_J} \]
\[ V_J \approx V_{OCC} \]
\[ I_{OUT} = \frac{V_{OCC}}{R_s} \text{ (SHORT CIRCUIT, } V_{OUT} = 0) \]

But, \( I_p \gg I_{OUT} \)

Therefore, \( I_D \approx I_p \)

---

Figure III-8. Current Limiting in Photovoltaic Cell Under Lightning Illumination

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current which is limited to the junction voltage divided by the series resistance. Therefore, most of the photocurrent generated flows through the junction \(I_0\) forward biasing the junction near open circuit voltage. For one photovoltaic cell to limit the current produced by a bypass group and become reverse biased, the shadowing must be so complete that the photocurrent produced is less than the current \(I_{OUT}\) actually flowing from the other cells in the bypass group which are not operating near short circuit. For example, at 100 times design illumination, the short circuit current typically increases by a factor of 5 to 10. Thus, a cell with 5 to 10 percent illumination would produce a photocurrent equal to the short circuit current of the fully illuminated cells. Therefore, the conditions which represent a reasonable worst case for normal illumination are an unlikely combination of conditions for lightning.

D. THERMOMECHANICAL

The possibility of the cell overheating and failing due to uniform power deposition is analyzed at the single cell level. Since the thermal resistance is an important design parameter and must be selected for a particular application, the results are given in terms of temperature rise relative to the temperature rise under open circuit conditions. Open circuit was chosen for reference, because electrical power is not flowing into or out of the cell and is independent of cell conversion efficiency. It is assumed that the temperature rise under open circuit and full design illumination must be determined for the particular application. Therefore, the temperature rise for other cell operating conditions are given in terms of this reference. Four operating conditions are considered (1) normal bias, that is, open circuit through short circuit with a resistive load, (2) reverse bias due to shadowing, (3) forward bias which would result from a load voltage higher than the open circuit voltage of a string driving current back into the array, and (4) the transient heating due to lightning.
Before reviewing the four operating regions, consider the simplified model of heat flow in a photovoltaic cell presented in figure III-9. Insolation power \( S \) flows into the cell at temperature \( T_C \). Under normal conditions electrical power \( P_O \) flows out of the cell. Assuming that all the heat emission mechanisms are reduced to a single thermal resistance \( R_{TH} \) and an infinite heat sink at temperature \( T_R \), the remaining power flows through the thermal resistance to the heat sink producing a temperature rise \( T_C - T_R \). Under open circuit conditions \( P_O = 0 \) and full design illumination \( S_R \), the temperature rise is the nominal temperature rise \( \Delta T_0 \) given by the product of design illumination times the thermal resistance. Failure of the cell will occur for \( T_C \) at or above 360°F (455°K) which is the melting point of solder.

1. Normal Operation Temperature Rise

Under normal operating conditions electrical power is being removed from the cell. When the cell is operating at either open circuit or short circuit either \( V_{OUT} \) or \( I_{OUT} \) are zero and the electrical power \( P_O \) is zero. Thus, open circuit and short circuit cause a temperature rise of

\[
\Delta T = S \times R_{TH}
\]

or

\[
\Delta T = \Delta T_0 \times S/S_R
\]

When the cell is biased at peak power, the maximum electrical power is removed and the electrical power is determined by the cell power conversion efficiency \( E \)

\[
P_O = E \times S
\]

and

\[
\Delta T = (S - ES) R_{TH}
\]

or

\[
\Delta T = \Delta T_0 \times (1 - E) \times S/S_R
\]
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\[ T_C = (S - P_0) \times R_{TH} + T_R; P_0 = I_{OUT} \times V_{OUT} \]

Open circuit temperature rise \( \Delta T_0 \) at design illumination \( S_R \)

\[ \Delta T_0 = T_C - T_R = S_R \times R_{TH} \]

Figure III-9. Simplified Model of Heat Flow in a Photovoltaic Cell
For a 13 percent cell conversion efficiency at full design illumination the temperature rise would be $0.87 \times \Delta T_0$. Since it is assumed that the array is designed to tolerate a temperature rise of $\Delta T_0$ above the worst case reference temperature, no problem will be encountered in the normal operating region, between open circuit and short circuit.

2. Reverse Bias Temperature Rise

Reverse bias can be caused by shadowing as discussed in sections B and C of this chapter. In reverse bias $V_{\text{OUT}}$ is negative and $I_{\text{OUT}}$ is positive, resulting in a negative electrical power ($P_0$). That is the electrical power is flowing into the cell. Two cases will be considered, first the ideal cell which has a very large shunt resistance and second a cell with the worst case shunt resistance such that the power dissipation in the cell is maximized. As shown in figure III-10 shunt resistance refers to the ohmic leakage current of a photocell between short circuit and reverse breakdown. Thus, the shunt resistance describes the slope to the reverse biased voltage versus current curve of a photocell, between zero voltage and reverse breakdown. These analyses assume the photocell does not go into reverse breakdown (avalanche breakdown), since cells can be permanently damaged by entering reverse breakdown. The design is expected to include bypass diodes as discussed in section C to limit the worst case reverse voltage.

For the ideal cell ($R_{\text{SHUNT}}$ is infinite) in reverse bias, but protected from reverse breakdown, the current is equal to the short circuit current ($I_{\text{SC}}$) of the shadowed cell at that illumination level. The electrical power at a constant reverse voltage ($V_R$) is as follows:

$$P_0 = I_{\text{SC}} V_R; \quad V_R < 0$$

The ratio ($K$) of short circuit cell current divided by the peak power cell current ($I_{pp}$) is very close to constant for single crystal silicon cells and typically varies from approximately 1.2 for flat plate cells to 1.06 for concentrator cells. Thus, electrical power can be rewritten in terms of peak power cell voltage ($V_{pp}$) and current ($I_{pp}$) or power conversion efficiency ($E$) as follows:

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Figure III-10. Simplified Photovoltaic Cell Electrical Model
\[ K = \frac{I_{SC}}{I_{pp}}; \text{ for silicon } 1.06 < K < 1.2 \]

\[ P_0 = K I_{pp} V_R = I_{pp} V_{pp} K V_R / V_{pp} \]

\[ V_{pp} I_{pp} = ES \]

\[ P_0 = ES K \frac{V_R}{V_{pp}} \]

Thus, the temperature rise for the ideal cell in reverse bias is given by

\[ \Delta T = (S - P_0) \times R_{TH} \]

\[ \Delta T = S (1 - E K V_R / V_{pp}) \times R_{TH} \]

\[ \Delta T = \Delta T_0 \times (1 - E K V_R / V_{pp}) \times S / S_R \]

By contrast, the nonideal cell in reverse bias will have current flowing due to both the photocurrent generated \((I_{SC})\) and the shunt resistance \((R_{SHUNT})\). Thus, the electrical power in reverse bias is as follows where the current in the shunt resistor is \(V_R\) divided by \(R_{SHUNT}\).

\[ P_0 = V_R \times (I_{SC} - V_R / R_{SHUNT}); \ V_R < 0 \]

Since the reverse bias of the shadowed cell is caused by the other cells in the series string, the combined current is limited to the short circuit current of the unshadowed cells operating at full design illumination \((S = S_R)\).

\[ I_{SC} - \frac{V_R}{R_{SHUNT}} < I_{SC^*} \]

\[ P_0 = V_R \times I_{SC^*} \]

\[ ^*S = S_R \]
Thus, using the same ratio (K) of short circuit cell current divided by peak power cell current (I_{pp}) and power conversion efficiency (E), the electrical power can be rewritten as follows.

\[ K = \frac{I_{SC}}{I_{pp}}; \text{ for silicon } 1.06 < K < 1.2 \]

\[ V_{pp}I_{pp} = ES \]

\[ P_0 = KI_{pp}V_R = KI_{pp}V_{pp}V_R/V_{pp} \]

\[ P_0 = KES_{R} V_{R}/V_{pp} \]

Thus, the temperature rise for the worst case nonideal cell in reverse bias is given by

\[ \Delta T = (S - P_0) \times R_{TH} \]

\[ \Delta T = (S - KES_{R} V_{R}/V_{pp}) \times R_{TH} \]

\[ \Delta T = \Delta T \times \left( \frac{S_{R}}{S_{R}} - KE \frac{V_{R}}{V_{pp}} \right) \]

The reverse bias temperature rise for both the ideal cell and worst case nonideal cell is plotted in figure III-11 for full illumination (S/S_R = 1) on the shadowed cell and half illumination (S/S_R = 0.5) on the shadowed cell. The horizontal axis represents the electrical power as a function reverse voltage normalized by the peak power voltage. The lower set of labels for the horizontal axis represents reverse voltage in a particular example where typical values are used for conversion efficiency, peak power voltage and ratio of short circuit current to peak power current. The difference between the ideal and nonideal cells is that the current in the ideal cell is proportional to insolation on the shadowed cell and the current in the nonideal cell is limited by the current in the illuminated cells which is not affected by the illumination on the
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\[ S/S_R = 1. \]

\[ S/S_R = 0.5 \]

\[ \text{NONIDEAL AND IDEAL} \]

\[ \text{NONIDEAL} \]

\[ \text{IDEAL} \]

\[ \frac{\Delta T}{\Delta T_0} \]

**EXAMPLE:** \( E = 13\%, K = 1.2, V_{pp} = 0.50V \)

\[ \rightarrow V_R \]

\(-25.V\) \(-20.V\) \(-15.V\) \(-10.V\) \(-5.V\) \(0.V\)

\( E = \) CONVERSION EFFICIENCY

\( K = \) SHORT CIRCUIT CELL CURRENT/ PEAK POWER CELL CURRENT

\( V_{pp} = \) PEAK POWER CELL VOLTAGE

\( V_R = \) REVERSE CELL VOLTAGE

\( \Delta T = \) TEMPERATURE RISE IN REVERSE BIAS

\( \Delta T_0 = \) TEMPERATURE RISE AT DESIGN ILLUMINATION AND OPEN CIRCUIT

\( S/S_R = \) SHADOWED CELL ILLUMINATION/ DESIGN ILLUMINATION

**Figure III-11. Temperature Rise in a Reverse Biased Photocell**

III-23
shadowed cell. The net effect is that the slope of the temperature versus reverse voltage curve is constant for the nonideal cell and is proportional to the illumination on the shadowed cell for the ideal cell.

The worst case nonideal cell and the ideal cell represent the limits on the response of a real cell. For full design illumination of the shadowed cell \((S/S_R = 1)\) which represents the worst case illumination, both the ideal and nonideal response are represented by the same line. Full design illumination on the shadowed cell is actually somewhat worse than any normal case in that shadowing causes reverse bias. If the cell were fully illuminated, then it would not be reverse biased. However, the amount of shadowing necessary to cause reverse bias has, in general, a complicated relationship with the operating conditions of the array.

As indicated by the example shown in figure III-6, reverse bias can be caused by a minor shadow (illumination of 75 percent of design illumination). For this reason, the case of full illumination on the shadowed cell is considered a reasonable worst case. Thus, the worst case relative temperature rise under reverse bias can be expressed by the following:

\[
\Delta T = \Delta T \times \left(1 - KE \frac{V_R}{V_{PP}}\right)
\]

3. **Forward Bias Temperature Rise**

Forward bias operation \((I_{OUT} < 0)\) of a photovoltaic cell can be caused by either of two conditions. First a transient produced by the load or electromagnetic coupling in the cables to the load can drive current back into the array as shown in figure III-12. Second shadowed cell(s) when connected in parallel with illuminated cells will not produce any current and will act like a load to the illuminated cells as shown in figure III-13.

In the case of partial shadowing in a parallel connection, the voltage of the combination will be no more than the average open circuit voltage of the individual cells. Thus, the current flowing in the shadowed cell will be no more than the current flowing within a photovoltaic cell.
Figure III-12. Load Transient Causing Forward Bias of Photovoltaic Cells

Figure III-13. Partial Shadowing of Parallel Photovoltaic Cells Causing Forward Bias of Shadowed Cell
under normal open circuit conditions. Since the shadowed cell is operating below full illumination, the power dissipated in the shadowed cell is lower than the power dissipated under open circuit and full design illumination. Thus, the temperature rise in the shadowed cell will be less than $\Delta T_0$.

Transients from the load or induced on cables between the load and the array may be kept out of the array by the use of blocking diodes as shown in figure III-14. The blocking diodes allow the normal current to flow into the load when the load voltage is lower than the array and block transient current from flowing into the array when the load voltage is higher than the array voltage. A voltage limiting device (such as a Zener diode, tranzorb, capacitor, etc.) would protect the blocking diode from damage. The voltage limiting device must have a high impedance at normal operating voltages, but conduct large currents below the rated breakdown voltage of the blocking diode. This configuration will keep load transients from entering the array. The voltage limiting device must be chosen on the basis of the normal operating voltage and expected transient magnitude/duration.

4. Heating Due to Lightning

The effects of lightning with respect to thermomechanical burnout for a forward biased cell will be considered. It will be shown that even for worst case, or near worst case conditions, the thermal effects of lightning will normally not cause failure. Only when high concentrations and high thermal resistances are used should the effects of lightning illumination be considered in the design of the system.

A lightning flash consists of several stages and lasts for several tenths of a second. Of interest are the return strokes of high current and short duration, the intermediate current as the trailing part of the return stroke which is a much more slowly decaying current at a fraction of the amplitude, and the continuing current, a low level, almost constant current of perhaps several hundred milliseconds duration. The intermediate and continuing current may or may not be present for any
Figure III-14. Blocking Diodes Protecting the Array From Load Transients
particular flash. Cianos and Pierce\textsuperscript{1} have compiled data on the physical characteristics of lightning, and have then modeled it for engineering usage. Their basic model of severe lightning will be considered here. This model closely resembles a lightning flash for which only 2 percent of lightning would be more severe. The parameters of interest for this model are given in table III-1.

**TABLE III-1. SEVERE LIGHTNING MODEL PARAMETERS**

<table>
<thead>
<tr>
<th></th>
<th>Current (kA)</th>
<th>Charge Transferred (Coulombs)</th>
</tr>
</thead>
<tbody>
<tr>
<td>RETURN STROKES</td>
<td>140 PEAK</td>
<td>28</td>
</tr>
<tr>
<td>INTERMEDIATE CURRENT</td>
<td>4 PEAK</td>
<td>20</td>
</tr>
<tr>
<td>CONTINUING CURRENT</td>
<td>0.4</td>
<td>120</td>
</tr>
<tr>
<td>FINAL STAGE CONTINUING CURRENT</td>
<td>0.2</td>
<td>32</td>
</tr>
</tbody>
</table>

A relationship is needed between current and optical power per unit area for a given ground distance from the lightning stroke. According to a U.S. Air Force report\textsuperscript{2} on lightning, the potential between cloud and ground just prior to discharge is estimated to be $10^8$ volts. Also it states that the conversion efficiency from electrical to optical power has been estimated to be 0.7 percent. Using these values and the 140 kA as peak current for a severe lightning stroke,


\[ P_{\text{optical}} = 0.007 P_{\text{electrical}} \]
\[ = 0.007 IV \]
\[ = 0.007 \times (140 \times 10^3 \text{ A}) \times (1 \times 10^8 \text{ V}) \]
\[ = 1 \times 10^{11} \text{ W} \]

This is in agreement with this same report which states that the optical power of lightning is expected to be in the range \(10^9\) to \(10^{11}\) watts.

The optical intensity in power per unit area at any distance can be obtained by integrating the contribution from each different segment of the stroke. Thus, for a 1-kilometer long stroke of \(10^{11}\) watts at a ground distance of 10 meters, the insolation will be \(1.24 \times 10^3\) kW/m\(^2\) or 1240 suns. This value of 1240 suns peak power for the 140 kA peak current gives a conversion factor of 8.86 suns/kA or 8.86 \(\times 10^{-3}\) sun-s/cm. From this, equivalent parameters for the severe lightning model can be calculated. They are given in table III-2. The computed duration is based on a rectangular pulse approximation.

| TABLE III-2. SEVERE LIGHTNING MODEL-EQUIVALENT PARAMETERS AT 10 METERS |
|-----------------|-----------------|-----------------|
| Power (Suns)    | Energy (Sun-s)  | Computed Duration (s) |
| RETURN STROKES  | 1240 PEAK       | 0.25            | 200 \(\times 10^{-6}\) |
| INTERMEDIATE CURRENT | 35 PEAK       | 0.18            | 5.1 \(\times 10^{-3}\) |
| CONTINUING CURRENT | 3.5           | 1.06            | 0.3               |
| FINAL STAGE CURRENT | 1.8           | 0.28            | 0.16              |
| TOTAL ENERGY 1.77 |

To determine the temperature rise of a cell, the thermal capacitance of the cell must be known. The specific heat of silicon\(^3\) is 760 J/kg/°C, and its density is 2.31 gm/cm\(^3\). Since the cell thickness ranges from 0.010 to 0.015 inches, the worst case of 0.01 inches will be used. Also, since 1 joule is W-s, and 1 sun is defined as 0.1 W/cm\(^2\), then the

thermal capacitance $C_{TH}$ can be calculated, viz.,

$$C_{TH} = \left( 0.76 \, \text{W-s/}^\circ \text{C} \right) \left( 2.31 \, \text{gm/cm}^3 \right) \left( 2.54 \, \text{cm/in} \right) \left( 0.01 \, \text{in} \right) \left( \frac{1}{0.1} \, \text{cm}^2\text{-sun/W} \right)$$

$$= 0.45 \, \text{sun-s/}^\circ \text{C}$$

The failure criteria will be a cell temperature of $455^\circ \text{K}$, the melting point of solder. A somewhat higher temperature is required to cause failure of the bulk silicon, PN junction or metalization.

Initially the assumption will be used that all the energy flows into the cell causing a temperature rise, and that none of this heat is removed, i.e., the thermal resistance to cool the cell is infinite. Then the temperature rise, $\Delta T$, will be given by

$$\Delta T = \frac{E_s}{C_{TH}}$$

where $E_s$ is the insolation energy in sun-s. From table III-2 the total energy of the severe lightning flash, $E_s$, is 1.77 sun-s. This gives

$$\Delta T = \frac{1.77}{0.45} = 3.9^\circ \text{C}$$

This is not a sufficient temperature rise to cause failure.

Now consider the case in which there is a 100X concentrator. This increases the energy incident on the cell by a factor of 100, which in turn increases the temperature rise by a factor of 100. The result is a $\Delta T$ of $390^\circ \text{C}$. Using a near worst case ambient temperature, $T_a$, of $315^\circ \text{K}$, the temperature $T$ of the cell is

$$T = T_a + \Delta T$$

$$= 315 + 390$$

$$= 705^\circ \text{K}$$

which is clearly a failure condition.
The assumption that the cell has no cooling is too severe for this case. However, a reasonable value of thermal resistance, $R_{TH}$, from the cell to ambient conditions, can be chosen so that the temperature rise will not cause failure.

To calculate $R_{TH}$, the allowed steady-state temperature increase, $\Delta T_{SS}$, above ambient for normal operation must be determined. Some of the trade-offs to consider are the decrease in output power and reliability as the temperature increases versus the increased cost of cooling. Since the output power is approximately proportional to the open circuit voltage, $V_{OC}$, $\Delta T_{SS}$ can be determined for any given output power degradation. $V_{OC}$ at 315°K is approximately 0.5 volts, and a reasonable value for the temperature coefficient of $V_{OC}$ is $-2$ mV/°C. This gives

$$\Delta T_{SS} = 2.5^\circ C \text{ for each } 1\% \text{ output power decrease.} \quad (\text{Eq. III-1})$$

Because of the 100X concentrator, there will be 100 suns incident on the cell under normal operation, giving $R_{TH}$

$$R_{TH} = \frac{2.5^\circ C}{100 \text{ suns}}$$

$$= 0.025 \frac{^\circ C}{\text{sun}} \text{ for each } 1\% \text{ power output decrease.} \quad (\text{Eq. III-2})$$

Before considering the value of $R_{TH}$ to be used, the equation for $\Delta T$ will be derived. The lightning will be treated a four rectangular pulses corresponding to those in table III-2. The equivalent circuit is given here.

![Equivalent Circuit Diagram](image-url)
where

\[ S(t) = \text{Insolation as a function of time.} \]

The differential equation is

\[ \frac{dT}{dt} + \frac{T - T_A}{R_{TH}C_{TH}} = \frac{S(t)}{C_{TH}} \]

\( S(t) \) will be considered a constant \( S \) for \( 0 \leq t \leq t_1 \). The solution for \( \Delta T \) is

\[ T = S R_{TH} + T_A + C_1 e^{-t/R_{TH}C_{TH}} \]

But the temperature at the beginning of each interval, \( T_0 \), which defines \( C_1 \) is known.

\[ T_0 = S R_{TH} + T_A + C_1 \]
\[ C_1 = T_0 - S R_{TH} - T_A \]

Thus,

\[ T = T_0 + (S R_{TH} + T_A - T_0) \times \left(1 - e^{-t/R_{TH}C_{TH}}\right) \quad \text{(Eq. III-3)} \]

Two cases of thermal resistance will be considered corresponding to 10 percent and 20 percent power degradation relative to the power at the ambient temperature. A 10 percent power degradation at 1 sun terrestrial and a concentration of 100 times give a thermal resistance of 0.25°K/sun (using equations III-1 and III-2). Under the same conditions, a 20 percent power degradation gives 0.50°K/sun. Evaluating equation III-3 gives the temperature of the cell at the end of each interval of the lightning as listed in table III-3. The temperature for the lower thermal resistance peaks at 431°K for the end of the intermediate current and is below the failure level of 455°K. The continuing current does not supply
TABLE III-3. CELL TEMPERATURE DURING LIGHTNING FOR TWO THERMAL RESISTANCE AND 100 X CONCENTRATION

<table>
<thead>
<tr>
<th>LIGHTNING PHASE</th>
<th>( R_{TH} = 0.25\degree K/\text{SUN} )</th>
<th>( R_{TH} = 0.50\degree K/\text{SUN} )</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>( T_0 ) (\degree K)</td>
<td>TEMPERATURE AT END&lt;br&gt;OF INTERVAL, ( T(\degree K) )</td>
</tr>
<tr>
<td>RETURN STROKE</td>
<td>340.*</td>
<td>395.</td>
</tr>
<tr>
<td>INTERMEDIATE CURRENT</td>
<td>395.</td>
<td>431.</td>
</tr>
<tr>
<td>CONTINUING CURRENT</td>
<td>431.</td>
<td>428.</td>
</tr>
<tr>
<td>FINAL STAGE CURRENT</td>
<td>428.</td>
<td>395.</td>
</tr>
</tbody>
</table>

*ASSUMING SUN IS SHINING, CAUSING \( \Delta T = 25\degree K \) OR \( 50\degree K \), AND AMBIENT TEMPERATURE IS \( 315\degree K \).
enough power to the cell to maintain the temperature and the cell begins to cool. The higher thermal resistance does not reach peak temperature until the end of the continuing current at 518ºK which indicates failure.

These results point out that lightning will not normally cause failure. However, for high levels of concentration and high thermal resistance, the possibility of such failure may need to be considered particularly in the design of the cooling system.
CHAPTER IV
PERFORMANCE OPTIMIZATION

Once the basic module has been designed and protected, and found to be compatible with the basic series parallel pattern, the next step is to optimize the performance of the array by determining the most efficient series-parallel pattern and by careful placement of blocking diodes and additional bypass diodes. Figure IV-1 shows the Design Flow for performance optimization. The previous design results which act as constraints for this phase are shown as inputs to the process.

The performance optimization discussed in this chapter refers only to electrical considerations, whereas the cost of the power generated is also an important constraint. Cost trade-offs are not considered within the scope of this contract. However, areas in which costing plays an important role have been identified and the impact qualitatively addressed.

A. SERIES-PARALLEL TRADEOFFS RESULTING FROM PARAMETER VARIATIONS

Some of the factors affecting the array design with respect to series-parallel considerations are the parametric variations of the cells making up the array. These will be considered here, along with some guidelines on how to use this information in determining a reasonable series-parallel configuration. The goal is to achieve the maximum output power for the array. To do this ideally, each cell should be operated at its maximum output power point. This, of course, is not possible due to the parametric variations from cell to cell.

Considering the forward biased I-V characteristics of the cells, it is the current and voltage at the maximum output power point which is of interest. These values are approximately proportional to the short-circuit current \( I_{SC} \) and open-circuit voltage \( V_{OC} \). Of interest now are the actual cell parameters which most directly affect \( I_{SC} \) and \( V_{OC} \). \( I_{SC} \) is straightforward, because the photocurrent, \( I_p \), is essentially
Figure IV-1. Design Flow for Performance Optimization
identical to $I_{SC}$. However, there is no parameter which is so related to $V_{OC}$. It can be shown that

$$V_{OC} = \frac{MKT}{q} \ln \frac{I_p}{I_s T^P e^{a/T}}$$  \hspace{1cm} (Eq. IV-1)

where

- $I_s$ = Saturation Current Constant in A/°K$^P$
- $a$ = Temperature Coefficient in °K
- $P$ = Exponent of Temperature
- $T$ = Temperature in °K
- $M$ = Emission Constant
- $q/K$ = Electron Charge/Boltzmann Constant in °K/V
- $I_p$ = Photocurrent in A

Two of these variables, viz., $I_s$ and $T$, will be allowed to vary independently to vary $V_{OC}$. (The parameter $M$ can also vary from cell to cell, but $I_s$ and $M$ cannot vary independently. Therefore, the data were reduced using an average value for $M$ and only assuming varying values for $I_s$. This technique is discussed in detail in the PV-TAP Users Guide, Vol. II, Section II-B.)

To come up with some realistic parameters, data from 40 actual cells were reduced. Using PV-TAP the parameter of interest was varied according to actual value, while the remaining parameters for each cell were all set to their average values. To check the validity of this while allowing only $I_s$ to vary, the resulting $V_{OC}$ distribution was compared with the actual $V_{OC}$ distribution of the 40 cells. They were in close agreement.

In considering the other variable, $T$, it can be shown that $V_{OC}$ versus $T$ is nearly a linear relationship, with the resulting $V_{OC}$ temperature coefficient being roughly -2 mV/°C. $I_{SC}$ will also vary with $T$, but this is small compared to the variations due to $I_p$, and will therefore not be considered here.
It should also be noted that $V_{OC}$ will vary with $I_p$, but this effect is small compared to $I_S$, since the relative variation of $I_p$ is much less than $I_S$. (See equation IV-1.) Therefore, the effects of $I_p$ on $V_{OC}$ will also be ignored here.

The approximations can then be made that

1. $I_{SC}$ is only a function of $I_p$ ($I_{SC} = I_p$).
2. $V_{OC}$ is only a function of $I_S$ or $T$ (equation IV-1).

It is of interest now to determine which parameter will cause a decrease in output power for any particular array configuration. This decrease is defined as the difference between the maximum output power for the array and the sum of the maximum possible output powers of the individual cells. Using the parameter values for the 40 actual cells, two arrays were considered using the PV-TAP program. These consisted of all 40 cells either in series or in parallel. The output from PV-TAP included the maximum output power for the array, with the corresponding output power for each cell. Also included was the maximum possible output power for each cell.

From these data the results given in table IV-1 were derived. The value given each parameter was the average value for all cells, except the one variable parameter, which was distributed in a gaussian fashion. Its mean and standard deviation were calculated from the actual values of the 40 cells. Note that $I_{SC}$ distribution is the same as $I_p$ since they are essentially the same, whereas $V_{OC}$ distribution is not the same as $I_S$ distribution, but is determined by the relationship as given in equation IV-1. Also note that the power degradation is essentially the same for the same relative deviation of either $I_{SC}$ or $V_{OC}$.

The qualitative aspects of the results are what would be expected. That is, if $I_{SC}$ varies in a series array where the current is constrained to be the same, all cells cannot be operating at their maximum output power current. Likewise, if $V_{OC}$ varies in a parallel array where the voltage is constrained to be the same, all cells cannot be operating at their maximum output power voltage.
Next, the effects of a temperature difference across an array will be considered briefly. It will be assumed that $I_S$ and $I_P$ are constant, and only temperature is causing a variation in $V_{OC}$. It is of interest to find the temperature distribution which gives the same $V_{OC}$ distribution as in the example of the 40 cell array, and consequently a 0.7 percent power degradation. $V_{OC}$ was approximately gaussian with a standard deviation of 18 mV. From the approximate temperature coefficient of $-2 \text{ mV} / \text{°C}$, the standard deviation for the equivalent temperature distribution would be $9\text{°C}$. However, a gaussian distribution for temperature may not be realistic, but a uniform (rectangular) distribution may be. Consider the case of an actively cooled array where the cooling fluid becomes warmer as it flows from one end of the array to the other. With this type of distribution, a maximum temperature difference of $30\text{°C}$ would give approximately the same standard deviation of $9\text{°C}$.

Factors used to determine whether an array should be built by starting with a series or parallel string of cells are the relative variations of $I_{SC}$ and $V_{OC}$. If $I_{SC}$ has the greater relative variation, the array should be built on a parallel string of cells; if $V_{OC}$ (from both $I_S$ and temperature variation) has the greater variation, then a serial string should be the base. The results will be less power loss, and an averaging of these parameters so that the effect of their variation on the next stage of the array (paralleling serial strings, or serializing parallel strings) will be greatly reduced. Based on the small sample of
Solarex flat plate cells, the power loss due to parameter variation is small for either series or parallel connection. However, a temperature gradient across a collector can increase $V_{OC}$ variations providing an advantage to serial connection.

In addition to these electrical trade-offs, cost can play an important role in selection of the optimum series-parallel pattern. For example, the number of bypass diodes used in the array can be reduced by using parallel connection of cells as the basic unit. The only criteria for placement of bypass diodes for cell protection is the maximum number of cells which can safely be connected in series to prevent overvoltage on a single cell. Connecting cells in parallel before serializing will not increase the cell vulnerability because the voltage is not affected by paralleling.

There are other considerations, as discussed in section IV-C for determining series-parallel wiring patterns. They all need to be considered together, in light of the objectives, to determine an optimum design.

B. **BYPASS AND BLOCKING DIODE PLACEMENT**

It was noted in chapter III that bypass diodes can be used for cell protection. Once the cells have been protected, additional bypass diodes can be positioned to improve performance. The additional bypass diodes reduce the detrimental effects of parameter tolerance, shadowing, and cell failure. The addition of diodes in blocking positions can also improve performance. Too many bypass and blocking diodes, however, can reduce output and cost effectiveness. The use of these diodes to optimize performance is discussed below.

1. **Bypass Diodes**

   In a given series string, shadowing of a single cell can present an open circuit to the rest of the string. The output of the entire string can be lost. If the string contains a bypass diode, shadowing will cause the string to go into bypass. The voltage of the string will be lost and an additional voltage drop will occur across the bypass diode. This condition is illustrated in figure IV-2(a). If more bypass diodes are used (as in b and c), the performance is improved
Figure IV-2. Effect on Performance of Addition of Bypass Diodes for One-Cell Shadowing
because less and less of the string is in bypass. The voltage of the string, $V_S$, will be the average voltage per cell times the number of cells in series minus the number of cells bypassed minus one bypass diode voltage drop.

$$V_S = \frac{m - 1}{m} nV_{\text{AVG}} - V_b$$

where $n$ = number of series cells
$m$ = number of bypass diodes
$V_{\text{AVG}}$ = average voltage per cell
$V_b$ = bypass diode forward voltage

It would appear from this scheme that the optimum situation would be to bypass every cell. This is not correct. In addition to the obvious cost penalty of implementing so many bypass diodes, consider the condition illustrated in figure IV-3 in which more than one cell is shadowed. For $n/3$ cells shadowed in a single bypass group, the results are the same as in figure IV-2(a). The improvement in splitting the string into two bypass groups is the same as in figure IV-2(b). Increasing the number of bypass groups to four does not yield any improvement; rather, it reduces the voltage by another bypass diode voltage drop. The general equation for the voltage as a function of the number of cells shadowed and the number of evenly spaced bypass diodes is

$$V_S = \frac{m - \text{ROUNDUP}(fm)}{m} nV_{\text{AVG}} - \text{ROUNDUP}(fm) x V_b$$

where $m$ = number of evenly spaced bypass diodes
$n$ = number of cells in series
$f$ = fraction of cells shadowed
ROUNDUP(fm) = number of bypass groups in bypass condition
$fm = \frac{fn}{n/m} = \text{number of cells shadowed divided by number of cells in each bypass group}$
ROUNDUP = increase to next higher integer
$V_{\text{AVG}}$ = average voltage per cell
$V_b$ = bypass diode forward voltage drop
Figure IV-3. Effect on Performance of Addition of Bypass Diodes for Multi-Cell Shadowing
Very little can be said about optimizing the design against random shadowing. If distributions of shadow sizes due to clouds, airplanes or other causes can be generated, an optimum spacing may be calculable. This would at best be a tedious task and at worst would not provide any significant improvement. The prime concern might well be the cost of implementing bypass diodes beyond the number required for protection.

For recurrent shadows, such as might be caused by collector end effects or nearby structures, maximum efficiency would generally be obtained by spacing bypass diodes so that no more than one bypass group is in bypass due to the shadow. In some cases, it might be desirable to deviate from even spacing in such a manner that extra bypass diodes are used only across those cells that are shadowed. Consider an example in which protection criteria require bypass diodes every 20 cells, but up to eight cells of some strings are shadowed due to a nearby structure. It would then be desireable to bypass the last eight cells in each of these strings with one or two diodes depending on the propagation pattern of the shadow and the cost per efficiency improvement of implementing these diodes.

The voltage obtained using this type of bypass scheme would be

\[ V_S = (1 - f)n V_{AVG} - m V_b \]

where
- \( n \) = number of cells in series string
- \( f \) = fraction of cells in shadow
- \( V_{AVG} \) = average voltage per cell
- \( m \) = number of bypass diodes in shadowed group
- \( V_b \) = forward voltage drop of bypass diode

In the case of collector end effects (as illustrated in figure IV-4), bypass diodes could be used to improve efficiency during end shadowing. However, the cost of the additional diodes beyond the number required for protection must be weighed against the impact of removing PV cells from the ends of the receiver tube or of lengthening the parabolic trough to reduce end effects.
FIGURE IV-4. BYPASS DIODES TO REDUCE END EFFECTS
2. Blocking Diodes

When series-connected strings of cells or modules are paralleled, blocking diodes can sometimes be used to improve performance. The blocking diode may be useful when several cells in a series string are shadowed (as illustrated in figure IV-5). Not only does this string produce no output, but if no blocking diodes are used, this string could also drain some of the current from the other strings, further reducing the current and voltage to the load. If blocking diodes are used, the loss may be reduced because no current can flow into the unproductive string. The output voltage will be reduced, however, by the forward voltage drop of the blocking diode in each string. This voltage loss occurs under normal operation. Therefore, any improvement in performance during shadowing could be offset by the loss in performance during normal operation. Even during shadowing, the losses due to blocking diodes could be greater than the loss without blocking diodes. A rough estimate of the trade-off in using blocking diodes is derived below.

Some assumptions and limitations should first be considered.

(1) Since blocking diodes are in series with the PV cells and the forward voltage subtracts from the voltage of the cells, the voltage of the cells in series, $V_S$, must be much greater than the forward voltage, $V_f$, of the blocking diodes. Thus, for $n$ cells in series,

$$V_S = n V_{MP} >> V_f$$

where $V_{MP}$ is the voltage of the individual cells at the maximum (peak) power point. It should be obvious that if the basic array building block is composed of parallel-connected PV cells, blocking diodes cannot be used in the basic module.

(2) Blocking diodes are placed on series strings when they are paralleled. But then, the subarray consisting of paralleled strings may be connected in series with other similarly connected subarrays (as illustrated in figure IV-6). There are $n$ cells...
Figure IV-5. Effects of Blocking Diodes on Voltage and Current
Figure IV-6. Schematic for Estimating Blocking Diode Trade-offs
in series, m strings in parallel and k subarrays in series. If one string is shadowed, the whole subarray, P1, could become reverse-biased, since in this condition the subarray is similar to a single cell in a series string whose Ip value is lower than the rest. If the subarray is reverse-biased, the blocking diode is not needed. Thus, for the blocking diode to be useful, the subarray must remain forward-biased. This can only be achieved if the short circuit current of the remaining m-1 strings, (m-1)ISC, is greater than the normal peak power current, IMP, of the other subarrays. Thus, (m-1)ISC > mIMP. Since IMP ≈ 0.9 ISC,

\[
\frac{m-1}{m} \geq \frac{IMP}{ISC} = 0.9
\]

Therefore, m > 10. Actually, m must be even greater than this since the voltage of the subarray must be not only nonnegative but greater than Vf.

(3) Current will not be drained from the m-1 strings into the shadowed string and thus, no blocking diode needed, unless the subarray voltage, Vp1, remains greater than the voltage of the shadowed string, VS1. Since the unshadowed cells in the shadowed string will be forced into open circuit, their combined voltage, VOCS, must be less than the voltage of the other unshadowed strings, VS.

\[
V_{OCS} < V_{S} = nV_{MP}
\]

Since VMP ≈ 0.8 VOC for a given cell, the number of shadowed cells in the string, nsh, is given by
\[(n - n_{sh}) V_{OC} < n(0.8 V_{OC})\]

\[n_{sh} > 0.2 n\]

Therefore, at least 20 percent of the cells must be shadowed. Actually, more than this must be shadowed since the voltage of the subarray will drop below \(nV_{MP}\).

With these assumptions in mind, consider the schematics in figure IV-5. With no blocking diodes, the power lost during shadowing will be the loss of string \(S1\) plus the power lost from the other strings into \(S1\). In a worst case situation, the voltage of \(P1\) remains at \(nV_{MP}\) while all of \(S1\) is shadowed. To induce a voltage on \(S1\) of \(nV_{MP}\), an amount of current equal to the short circuit current minus the peak power current of one string must be forced through the shadowed string. Therefore, the power lost without blocking diodes is given by

\[
P_{LWOBD} = I_{MP} nV_{MP} + (I_{SC} - I_{MP}) nV_{MP}
\]

With blocking diodes, the power lost during shadowing will be the loss of the string \(S1\) plus the loss due to using blocking diodes in \(P1\) and all the other \(k-1\) subarrays.

\[
P_{LWBD} = I_{MP} nV_{MP} + (m - 1) I_{MP}V_f + (k - 1) m I_{MP}V_f
\]

To guarantee the usefulness of blocking diodes

\[P_{LWBD} < P_{LWOBD}\]

Substituting the expressions and eliminating the identical first terms in each yields

\[(m - 1) I_{MP}V_f + (k - 1) m I_{MP}V_f < (I_{SC} - I_{MP}) nV_{MP}\]
Since, \( I_{MP} = 0.9 I_{SC} \)

\[
[(m - 1) + (k - 1)m] I_{MP} V_f < (I_{MP}/9) nV_{MP}
\]

Eliminating \( I_{MP} \) from both sides of the equation and assuming \( V_f \approx V_{MP} \), which is generally optimistic.

\[ n > 9(mk - 1) \]

For \( m = 10 \) or \( 11 \), the number of cells in each string which determines the ratio \( V_S/V_f \) is given for \( k \) subarrays in series in table IV-2.

| TABLE IV-2. NUMBER OF CELLS REQUIRED IN SERIES STRING VERSUS NUMBER OF SUBARRAYS |
|---|---|---|
| \( n \) | \( m = 10 \) | \( 11 \) |
| \( k = 2 \) | 171 | 189 |
| 3 | 261 | 288 |
| 4 | 351 | 387 |
| 5 | 441 | 486 |

Since this is a conservative estimate of \( n \), it can be seen that blocking diodes are only marginally useful for \( k > 1 \) and then only for \( m > 10 \) and \( n > \) the values shown.

The condition \( k = 1 \) occurs when the total array is completed by connecting subarrays in parallel. This case is not covered by the above table since the condition \( m > 10 \) was specified based on \( k > 2 \).

In this case, the expression reduces to the following.

\[ n > 9 (m - 1) \]
To illustrate the significance of these expressions consider two examples. For both examples, assume the output voltage of the array is at a particular level within the typical range of 200 V to 450 V. The first example uses flat plate cells with peak power at 1 amp and 0.5 volts. Thus, for a 100 kW array, the ratio of n divided by m is between 0.8 (400/500) at 200 V and 4.1 (900/220) at 450 V. For larger arrays the ratio would be lower. Therefore, since \( n < 9 \) (\( m - 1 \)), even with \( k = 1 \), blocking diodes would never improve performance. However, blocking diodes may be required for protection.

The second example uses concentrator cells with peak power at 40 A and 0.5 V. Thus, for a 100 kW array with \( k = 1 \), the ratio of n divided by m is between 32 at 200 V and 163 at 450 V. Therefore, for high currents per string or multiple strings per blocking diode, blocking diodes can under certain shadow conditions improve performance. However, the losses due to blocking diodes are present all the time, but the conditions where performance is improved by blocking diodes is intermittent. Therefore, the user must evaluate the efficiency of using blocking diodes for performance improvement for his particular case. If, for example, the final aggregation consists of paralleling (\( k = 1 \)), and m is small (e.g., 4 strings), then, the use of blocking diodes (in this case, only 4) is certainly warranted.

C. EFFECTS OF SHORTED AND OPEN CELLS ON PERFORMANCE

When a cell fails either short or open, the power output of that cell is lost. The failure can sometimes cause greater losses, however, than just the power of the one cell. The amount of power loss depends on the method of connection of the cell and the placement of bypass diodes. Since there are two possible interconnection methods for individual cells, series or parallel, four conditions must be considered. The power loss for each condition is outlined in table IV-3. Each will be discussed in turn.
TABLE IV-3. POWER LOSS DUE TO SHORTED AND OPEN CELLS

<table>
<thead>
<tr>
<th>INTERCONNECTION</th>
<th>CELL CONDITION</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>SHORTED</td>
</tr>
<tr>
<td>SERIES</td>
<td>LOSE POWER</td>
</tr>
<tr>
<td></td>
<td>OF CELL</td>
</tr>
<tr>
<td>PARALLEL</td>
<td>LOSE POWER</td>
</tr>
<tr>
<td></td>
<td>OF PARALLEL STRING</td>
</tr>
</tbody>
</table>

1. **Series Short**

When a series-connected cell fails short, the power loss of the series string is only the power of the one cell because it is the same as bypassing the cell with a wire. The voltage is lost but current will still flow.

If the series string is in turn connected in parallel with other series strings, there will be a slight decrease in the output voltage of the parallel combination due to the lower voltage of the string with the shorted cell. The overall effect is a power loss of about one cell.

2. **Parallel Short**

When a parallel-connected cell fails short, the power of the entire parallel string is lost because no voltage can be maintained across the terminals.

If the parallel string is, in turn, connected in series with other parallel strings, the output voltage of the series combination will be decreased by the voltage of one cell. The situation is similar to a shorted cell in a series string except that the power loss is greater because the current is greater by the number of cells in parallel.

3. **Parallel Open**

When a parallel connected cell fails open, the power loss of the parallel string is only the power of one cell because it is the same
as removing the cell or putting a blocking diode in series with a shadowed cell. No current is produced, but no current is drained from the other cells either.

If the parallel string is, in turn, connected in series with other parallel strings, the parallel string with the open cell will act like a series-connected cell that has a low photocurrent or is partially shadowed. The parallel string with the open cell could go into reverse bias. If it were part of a bypass group, the group could go into bypass. Thus, the power of the whole bypass group could be lost.

4. Series Open

When a series connected cell fails open, the power of the whole string (or bypass group) is lost because no current can be drawn from that string (or no voltage will be generated by the group in bypass).

If the series string is, in turn, connected in parallel with other series strings, the open string will have the same effect as if it were removed or as if a blocking diode were placed in a shadowed string. The situation is similar to an open cell connected in a parallel string except that the power lost is greater because the voltage is greater by the number of cells in series.

If the open string has bypass groups within it, the effect when the string is paralleled will be different. The string will not look like an open circuit because the bypass group with the open cell will be in bypass. The effect will be similar to the series string connected in parallel (described in paragraph 1) except that instead of losing one cell, one whole bypass group is lost plus the power lost in the bypass diode.

The effects of shorted and open cells on higher orders of aggregation can be deduced based on these guidelines.

The relative performance merits of series or parallel connection of cells in the cases of shorted or open cells can be summarized
as follows: In the case of shorts, series-connection of cells is more desirable since only the one cell is lost whereas shorts in parallel-connected cells cause the loss of the whole parallel string.

In the case of opens, there is also an advantage to series over parallel connection of cells. In the case of series connections, opens can cause the loss of a whole string or bypass group, but in the case of parallel connections, opens can sometimes cause the parallel string to go into reverse bias and the series bypass group of which the parallel string is a part to experience large voltage losses or go into bypass. The relative severity of the two cases is dependent on the number of cells in parallel and the number of parallel strings in series per bypass group. The trade-off can be evaluated by considering the power loss for each case.

If n cells are connected in parallel, the lowest loss will occur if a bypass diode is placed across each parallel string. Thus, the loss would be limited to the single string power plus the bypass diode power.

\[
P_{LPS} = V_{MP} (nI_{MP}) + V_b (nI_{MP})
\]

\[
= nI_{MP} (V_{MP} + V_b)
\]

where \(P_{LPS}\) = power loss of parallel string
\(V_{MP}\) = voltage of cell at maximum power point
\(I_{MP}\) = current of cell at maximum power point
n = number of cells in parallel
\(V_b\) = forward voltage of bypass diode

If m cells are connected in series within a bypass diode, the power lost if one cell opened would be

\[
P_{LSS} = (mV_{MP}) I_{MP} + V_b I_{MP}
\]

\[
= I_{MP} (mV_{MP} + V_b)
\]
where $P_{LSS}$ = power loss of series string
$m$ = number of cells in series
and other variables are as defined above.

If parallel connection of cells is to be more advantageous than series connection,

$$P_{LPS} < P_{LSS}$$

$$nI_{MP} (V_{MP} + V_b) < I_{MP} (mV_{MP} + V_b)$$

$$n < \frac{mV_{MP} + V_b}{V_{MP} + V_b}$$

For a typical case, if $m = 10$, $V_{MP} = 0.5V$ and $V_b = 1.0V$, $n$ must be less than 4 cells. Therefore, more bypass diodes must be used for paralleling cells than for cells in series to equalize the power losses for each case.

Therefore, by serializing cells, power loss is minimized in the case of shorted cells and cost of bypass diodes is minimized in the case of open cells. Furthermore, based on limited data, cell failures tend to be dominated by short circuits rather than open circuits.
BIBLIOGRAPHY


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