CIRCUIT DESIGN CONSIDERATIONS*
FOR PHOTOVOLTAIC MODULES AND SYSTEMS

C. Gonzalez and R. Weaver**
Jet Propulsion Laboratory
California Institute of Technology

ABSTRACT
As part of the Jet Propulsion Laboratory's Low-Cost Solar Array Project, a program of module and array circuit-design studies has been carried out to improve the reliability of modules and to develop strategies for improving array system fault tolerance. Analyses to determine optimum element configuration and circuit design strategies, made with the use of a computer model that uses the measurable characteristics of cells and modules as input, are described and results are presented.

Guidelines for implementing strategies to deal with specific module and array system circuit-design problems, involving use of series-parallelizing and bypass diodes to reduce module and array system power losses resulting from anomalies, are offered. Several different power-loss conditions resulting from anomalies are considered.

INTRODUCTION
Certain faults occur in terrestrial photovoltaic modules, both at beginning of life and throughout field experience. These faults occur as a result of initial mismatch of photovoltaic cell characteristics, and of environmentally induced stress or stress induced during maintenance in the field. In addition to mismatch, causes include open-circuit cell interconnects and cracked cells. One failure mechanism that can cause severe cell cracking is hail impact. Cell failure can also be caused by uneven shading of cells.

The objective of the task described here is to investigate the effectiveness of certain circuit-design strategies in ameliorating the effects of faults on modules and on array-system performance. The task has yielded a set of guidelines for incorporating appropriate strategies into module and array-system circuit designs. The objective of the guidelines is to maximize the reliability of modules and arrays by developing fault-tolerant circuitry.

Nomenclature
Definitions and nomenclature to be used in the discussion are presented in Figure 1. A photovoltaic module consists of solar cells electrically connected in series and/or parallel. A string of cells connected in a pure series arrangement is referred to as a series string or substring. When series strings are wired in a parallel configuration, they are called parallel strings and a group of parallel strings connected at their end points is called a series block. Modules are grouped together in panels for structural purposes, forming an array. A branch circuit is composed of a group of series blocks between the positive and negative termination points of a power conditioner. Therefore, an array is a collection of branch circuits. The series blocks may be whole modules or parts of modules. In the former case, series blocks are connected together through connectors external to the modules; in the latter, some series blocks are connected by internal module wirings, while groups of series blocks are connected externally. No distinction is made in the type of connections involved in this discussion.

Circuit Design Strategies

Two important circuit design strategies are...
considered in the task. The use of increasing numbers of series blocks and parallel strings per module and branch circuit as a circuit-design strategy, called series-paralleling, is accomplished by making cross-connections between parallel strings of cells after selection of the appropriate number of parallel strings. These cross-connections are also called cross-ties.

The second circuit-design strategy considered is the use of bypass diodes. A bypass diode is connected in parallel with a given number of series blocks. The bypass diode does not conduct unless the voltage across the series block is reversed from normal polarity by a small amount, usually 0.5 V. Then the diode passes virtually unlimited current at its operating voltage in the range of interest of this study. The purpose of using a diode is to prevent the series block in question from operating at a high reverse voltage; in this state it absorbs power from the system, and cells operating with reversed polarity become hot, leading to physical degradation of cell and module. This condition is called back-biasing; its result is termed the hot-spot problem, from the fact that cells do not heat uniformly, but develop local hot-spots.

A series block or individual cell can become back-biased from several causes. The open-circuiting of one or more cells or series strings in a series block can cause the series block to operate at a current level that reverses its voltage. The same thing happens to a cell when it cracks, taking active surface area from the circuit. In fact, a cell can be considered as a sum of parallel elements: loss of one element is analogous to loss of a cell string in a series block.

Another cause of back-biasing is the non-uniform shading of cells or series blocks. Those that are shaded to a greater degree than the rest of a module or branch circuit will be back-biased.

Each circuit design strategy has advantages and disadvantages. Two of the factors that must be considered are:

1) Cost of implementing the technique versus gain in module performance and reliability.

2) Gain in the area of concern, such as power, may be vitiated by worsening of the situation in another area, such as hot-spot heating.

**ANALYTICAL APPROACH**

The approach used in the task involves the use of a computer model with appropriate statistical analyses. The computer model calculates cell and module I-V curves based on the following equation:

\[
I = I_{sc} \left( 1 - e^{0.87 \times \text{FF}} \right) \left( \frac{V - V_{oc}}{V_{oc}} - 1 \right) - \frac{V}{R_{sh}}
\]

where:

- \( I \) = current of element at voltage \( V \)
- \( I_{sc} \) = short-circuit current
- \( \text{FF} \) = fill factor
- \( V_{oc} \) = open-circuit voltage
- \( R_{sh} \) = shunt resistance

The photovoltaic parameters are those commonly measured for cells and modules.

The computer model simulates various circuit designs with and without bypass diodes by adding the I-V curves of the component elements. An element is any cell or combination of cells located in a module or branch circuit. Failures can be introduced by adding I-V curves of the elements containing the types of failures being considered.

Because of the many elements involved in the typical multi-array system a statistical approach must be taken. There are two aspects to the requirements for a statistical treatment. First, a group of solar cells will have a statistical distribution of the characteristic parameters. The computer can select values of cell characteristic parameters from a given statistical distribution and assign them to the cell as it combines I-V curves.

Second, the locations of multiple failures are significant when the number of failures is not large enough to saturate the array system. Thus, the most likely location of multiple failures has an important effect on array performance. The statistical treatment of failure location has been performed in conjunction with the computer model but not internal to it. The output of the statistical model is used to define the number of cells most likely to fail for a given wiring configuration.

The output of the circuit-design computer model provides the I-V curve of the resultant combination of elements along with the maximum power of the combination. These results are combined with a statistical evaluation of the state of a given photovoltaic system to determine the most probable power output under given failure rates.

**MODULE AND SYSTEM PERFORMANCE CONSIDERATIONS**

Several different aspects of the performance of modules and arrays are considered in the following discussion of the methods used to determine the optimum circuit-design strategies to improve performance.
Mismatch Losses

The statistical distribution of cell parameters leads to electrical mismatch losses in modules. This occurs when cells (or series blocks) whose short-circuit currents vary considerably are combined.

The effect of mismatch is to limit the short-circuit current of the combination to a value closer to the low end of the distribution than to the average. This means that power available from the combination will be less than the sum of power of the individual cells. This is called a mismatch loss. Similar results would occur with elements combined in parallel based on open-circuit voltage. In practice these losses are not significant. Mismatch in fill factor is not important, since the mismatch averages out, producing no power loss.

A Monte Carlo analysis using the computer model, with I_{sc} values selected from a histogram distribution, was used to simulate mismatch losses in modules occurring before any field degradation. The only strategy relevant to this case is series-paralleling. Figure 2 is an example of mismatch loss as a function of the number of parallel strings and series blocks in the module. The short-circuit current distribution used is also given. Comparison of similar results indicates that mismatch losses are not significant for a histogram distribution having a half-width of 5% to 10%. As the short-circuit variation becomes more pronounced, losses become more significant. In this case increasing the number of parallel strings and series blocks in the module provides reduction of losses.

Manufacturing Yield

Another aspect of module performance is manufacturing yield, which is the fraction of modules coming off the assembly line and/or delivered at the site that are acceptable for use in the field. The yield is based on the amount of power deviation from an established average that is considered acceptable for a module. One way to increase yield is the use of series-paralleling, which was used in the analyses discussed here. Bypass diodes could also be used, and are discussed below in connection with array power loss.

Figure 3 gives a comparison of the values of module manufacturing yield obtained for different numbers of parallel strings and series blocks. In this case, a module cell failure rate of 1/1000 and an acceptable power deviation from average of 10% were assumed. As can be seen from the figure, series-paralleling has a significant effect.

Fault Tolerance

Another module and array system performance criterion is fault tolerance. Faults arise primarily from cell failures that, in turn, arise from cracking. These faults lead to array power degradation and heating problems.

The use of series-paralleling and bypass diodes is important in enhancing fault tolerance. To ascertain the effectiveness of various degrees of series-paralleling, the power output of an array under specific failure conditions must be determined for a variety of series-parallel configurations with varying numbers of diodes. Power loss varies inversely with degree of series-paralleling, but limits imposed by physical constraints, as well as those of cost and of thermal problems, make it impossible to achieve negligible power loss by means of unlimited series-paralleling. Thus a
number of configurations must be considered, and those offering acceptable power loss must be investigated in the light of the system constraints.

In the analysis described below, only open-circuit failures were considered. The analysis of the effects of failures on a large array system requires a complex statistical approach; in order to simplify it, only the statistics of the occurrence of open failures were considered. With the number of cells per substring decreasing to approach one, the results of an analysis for open cells become applicable to an array with partially failed cells: e.g., a series block of eight parallel substrings with one failed open can be treated the same as one of four parallel substrings and one cell 50% degraded. The consideration of only open failures allows the determination of branch-circuit power loss as a function of substring failure density independently of the number of cells per substring. In order to relate the results to a given array system, the appropriate cell failure density must be related to substring failure density.

Fault tolerance optimization at the module level is a relatively simple matter because modules cannot tolerate more than one or two failures without losing significant power. Analysis of an array system is far more complicated since it can contain many failures. The difficulty arises in locating the failures. Their locations can be defined in terms of the types of elements created: thus, a branch circuit can be described as containing $N_c$ cells per substring, $N_s$ series blocks, and $N_p$ parallel strings. Assuming that a branch circuit contains three open cells, several possibilities exist: one of these is the occurrence of all three failures in separate series blocks. In this case the branch circuit has one set of $N_s-3$ normal series blocks and three series blocks with one of $N_p$ parallel strings failed. Table 1 considers the spectrum of possible cases with three failures.

The probability of occurrence of each state of the array in Table 1 can be ascertained from a given distribution of failures. The I-V curves of the various states can be simulated by the computer model.

### Determination of Array Power Degradation

A method, developed to determine array power degradation, is described here. This method is meant to serve as a tool for array circuit designers to use in optimization studies.

The method applicable to various systems, must be used subject to a number of module and array constraints, leading to the requirement for parametric analyses. The parameters of concern include: module and branch circuit voltage level (cells per substring); cell fill factor; degree of series-parallelizing; number of bypass diodes used, and level of cell failures.

<table>
<thead>
<tr>
<th>Failure Location</th>
<th>No. of Normal Series Blocks</th>
<th>No. of Failed Series Blocks with $x$ Failed Substrings</th>
</tr>
</thead>
<tbody>
<tr>
<td>3 separate series blocks</td>
<td>$N_s$</td>
<td>3</td>
</tr>
<tr>
<td>2 separate series blocks</td>
<td>$N_s$</td>
<td>1</td>
</tr>
<tr>
<td>3 separate substrings</td>
<td>$N_s-1$</td>
<td>1</td>
</tr>
<tr>
<td>2 separate substrings</td>
<td>$N_s-1$</td>
<td>1</td>
</tr>
<tr>
<td>same substring</td>
<td>$N_s$</td>
<td>1</td>
</tr>
</tbody>
</table>

### Table 1. Possible Combinations of Series Blocks with a Given Number of Failed Substrings for Three Failed Cells

<table>
<thead>
<tr>
<th>Objective of Method</th>
</tr>
</thead>
</table>

The end result of applying this method is the generation of a family of curves giving array power degradation as a function of the number of series blocks and parallel strings per branch circuit. Power degradation is plotted against the substring failure density. An example of this is shown in Figures 4 and 5 for the case of eight parallel strings. The two figures allow a comparison of the results obtained with and without bypass diodes. Similar results have been generated for branch circuits with one, four and 16 parallel strings and for different diode placement.

Substring failure density was chosen as a determining parameter instead of cell failure density in order to limit the number of curves required. If cell failure density had been used, instead of one set of curves for each case illustrated by Figures 4 or 5, a separate set would have had to been developed for each branch circuit with a different number of cells per substring.

The appropriate substring failure density to be used, for a given array, in conjunction with Figures 4 or 5 is determined from the following equation:

$$F_{SS} = 1 - (1 - F_c) N_c$$

(2)
where:

- \( F_{ss} \) = substring failure density
- \( F_c \) = cell failure density
- \( N_c \) = number of cells per substring

The binomial distribution, which is given below, is used to determine the appropriate probabilities.

\[
f(x) = \frac{n!}{x!(n-x)!} p^x Q^{n-x}
\]  

where \( f(x) \) is the probability of the occurrence of \( x \) events in \( n \) trials, if the probability of occurrence of the event in any given trial is \( p \) and \( Q = 1 - p \), the probability of the event not occurring.

The degree of failure associated with the branch circuits in an array is the first determination made. This is measured by the number of failed substrings, \( x \), in a given branch circuit, and in turn, by the fraction of series blocks, \( F_x \), which have this number of failed substrings. The fraction of series blocks having different numbers of failed substrings is determined as a function of substring failure density. An example of this is shown in Figure 6.

The power loss associated with branch circuits having a given degree of failure is calculated. A starting point is the calculation of the power loss of a branch circuit where all failed series blocks have the same number of failed substrings. Figure 7 gives the branch circuit power loss for eight parallel strings as a function of the number of series blocks having 1, 2, ..., 7 failed substrings.

The branch circuit power loss for combinations of failed substrings at a given substring failure density is then determined. An example of the procedure follows. Consider a branch circuit having a fraction, \( F_x \), series blocks with \( x \) failed substrings and \( F_{x-1} \) with \( x-1 \) failed substrings. Assume \( F_x < F_{x-1} \). (If \( F_x = F_{x-1} \), the series blocks with \( x \) failed substrings dominate and power loss can be computed based on them.) This situation will lead to one of two possible cases. The first is the case in which the \( F_x \) series blocks dominate (similar to the case when \( F_x = F_{x-1} \)). The more difficult case to analyze occurs when the power loss due to the \( F_x \) series blocks is less than or equivalent (or slightly greater) to that with \( F_{x-1} \) series blocks. Since the values of \( F_x \) and \( F_{x-1} \) are based on a generalized case, caution must be used in specific cases when determining these fractions.

Consider the example of a branch circuit having 2000 series blocks with \( F_x = 0.005 \) and \( F_{x-1} = 0.0045 \). This branch circuit would have 10 series blocks with \( x \) failed substrings and 130 with \( x-1 \) failed substrings. The branch circuit power loss would be computed for 130 series blocks with \( x-1 \) failed substrings. A second value would be computed for 10 series blocks with \( x \) failed substrings, assuming that there are also 130 series blocks with \( x-1 \) failed substrings. This second power loss must be estimated for combinations of \( x \) and \( x-1 \) failed substrings. The curves used in doing this are similar to those shown in Figure 7.
The array power loss is determined by summing the power losses for branch circuits having one failed substring, a maximum of two failed substrings, and so on. In the summation each power loss is weighted by the fraction of branch circuits having series blocks (at least one) with a maximum of the corresponding number of failed substrings. In other words, this fraction of branch circuits will have series blocks with numbers of failed substrings up to and including the maximum.

Results of Method

The results, illustrated in Figures 4 and 5, can be used to develop guidelines for module and array circuit design. The actual curves used depend on the module and array design parameters, cited above, which act as constraints. These constraints will then define the minimum and maximum series-parallel configurations allowed, which in turn determine which and how many sets of curves are required. A cell-failure rate must be determined either based on experience with similar systems or on the most likely value.

Next those series-parallel configurations and diode placement which lead to acceptable system performance in terms of power degradation must be identified. Finally, those that are unacceptable from a hot-spot standpoint must be discarded as discussed below.

If a cell failure rate per year is defined, a plot of array power loss versus time can be made. Figures 8 and 9 provide a history of power loss over 20 years for an annual cell failure rate of one per 10,000. Shown for comparison, for the case of eight parallel strings, is the effect of using diodes which leads to a decrease in power degradation.

Curves such as those shown in Figures 8 and 9 facilitate identification of optimum circuit configurations based on operation over a given number of years. It also allows the option of determining a failure replacement policy and
consequently the array system life-cycle cost. These two questions are addressed in a companion paper presented by Dr. Ron Ross of JPL (1).

Hot-Spot Problem Determination

Although increasing the number of series blocks decreases power loss, this strategy by itself increases the hot-spot problem. The severity of the problem depends on certain cell characteristics and on the operating point of the system under question.

A simple technique can be used to determine the upper limit on the amount of energy absorbed by a group of cells in a back-bias condition. The circuit element in question can be considered as being composed basically of two parts. One part contains failed cells, either open failures or partial cell failures (cracked cells); the second part is composed of unfailed cells. Each part is composed of one or more series blocks. Figure 10 demonstrates the technique, applied with the entire element operating at short-circuit current conditions. This represents the worst-case field condition of a branch circuit being short-circuited for safety during maintenance, or a portion of a branch circuit inside a bypass diode. Since the entire element is operating at or near short-circuit conditions, the back-biased portion must be operating at a negative voltage whose magnitude is equal to that of the positive voltage of the unfailed portion. The exact operating voltage can be found by reflecting the I-V curve of the unfailed portion into the negative quadrant and determining the intersection of the two curves. This provides the voltage of the failed element. The product of this voltage and the operating current (essentially the short circuit current of the total element) gives the power absorbed by the failed element. That power drain will be distributed among all the cells carrying current.

A useful tool can be developed by drawing a family of curves representing the I-V curves of the failed and unfailed elements discussed above. The curves represent elements containing different numbers of parallel strings and series blocks as indicated in Figure 11. The absorbance is calibrated in terms of power absorbed per cell as a ratio of this power to the maximum power produced by an unfailed cell. Therefore, Figure 11 can be used to determine the power absorbed by the remaining cells in a series block of n substrings when one substring becomes open circuited. The intersection of the n parallel horizontal line with that vertical line representing the total number of series blocks involved gives the appropriate power ratio. If cracked cells are used, an approximate answer can be found by considering a cracked cell to be composed of parallel elements.

The slope of the horizontal lines is a critical factor (Figure 11). This slope is determined by the value of the shunt resistance of the cells in question. The curves shown in the figure were determined for a nominal value of 100 ohms. A change in this value of an order of magnitude is required to alter the slope appreciably. A larger value would flatten out the curve. Therefore, the most representative value of shunt resistance should be used in determining the existence of a hot-spot problem.

The most useful design strategy for reducing hot-spot problems is the use of bypass diodes. The hot-spot problem increases as the number of series blocks increases (Figure 11). Decreasing the number of series blocks in a branch circuit may be physically impossible; the smallest series block may be a module whose size is fixed. However, a bypass diode will remove all the series blocks in parallel with it if a back-bias situation occurs. It effectively reduces the number of series blocks of concern in Figure 11 to those in parallel with it. In addition, use of bypass diodes allows the acceptable number of series blocks to be increased for reduced power loss or other considerations. Adding diodes, when
CONCLUSIONS

Techniques have been described for evaluating the effects of different circuit design strategies on the fault tolerance of large terrestrial photovoltaic arrays. This has been accomplished by developing a generalized set of curves which can be adapted to a variety of array systems. The techniques required to generate the curves are somewhat complex but can be easily duplicated with the aid of a computer. The results obtained allow computation of the array power degradation as a function of cell failure rate for various circuit design configurations. It is also possible to find out if back-biasing occurring under a given configuration will lead to hot-spot problems.

As a result of analyses performed in the task some general guidelines can be given relative to circuit design strategies. Specific conclusions for a particular array can only be drawn after a careful analysis using the characteristic cell, module and array parameters. The general conclusions include the following:

1. The use of bypass diodes is the best circuit design tool to reduce power loss and hot-spot problems.

2. The paralleling of cell strings within modules is effective at reducing cell mismatch losses and increasing manufacturing yield.

3. The use of increased number of series blocks, although leading to reduced power loss, can exacerbate hot-spot problems and should be accompanied by the use of bypass diodes.

REFERENCES