ABSTRACT

Bypass diodes are often required to limit the potential for reverse voltage "hot-spot" heating in high voltage arrays or in arrays that undergo periodic operation near the short-circuit point. In addition, when properly applied, bypass diodes can minimize the effect of shadowing and various internal module failures on the array energy output. This paper discusses the mechanical and electrical integration of bypass diodes beginning with the array-level considerations which influence the selection of an implementation approach. Concepts for the mounting of these diodes, both internally within the module encapsulant and externally to the exposed rear surface of the module, are described. Factors affecting the reliability of bypass diodes, including the control of junction temperature through adequate heat sinking and the derating of reverse voltage, are discussed.

INTRODUCTION

Diodes perform two important functions in photovoltaic modules and arrays. When applied in a bypass mode, those diodes can shunt source circuit current around defective or shadowed circuit elements thus limiting both the power loss due to these conditions as well as the potential for reverse voltage "hot-spot" heating of solar cell circuit elements within the affected area. In a blocking or circuit isolation application, diodes can be used to prevent reverse current through an individual source circuit which has a lower voltage capability than other power sources on the same dc bus. In either of these applications, the diode must be mounted and packaged to limit the junction temperature to an acceptable level while conforming to industry standards for product safety when deployed in the field for the design life of the system.

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Circuit layout is such as to provide adequate "hot-spot" heating immunity without the use of bypass diodes, then the option pictured in Figure 1(a) becomes a valid design approach. The incorporation of a single bypass diode across the module terminals, whether internally or externally mounted as shown in Figures 1(b) and (d), is not regarded as a reasonable action by the module designer since its use does not enhance the ability of that module to survive the "hot-spot" heating exposure and complicates the array circuit design by introducing problems of current sharing among individual module diodes if the array designer wishes to employ a parallel-connected group of modules as a circuit element. Depending on the module circuit configuration, it may be necessary to employ multiple bypass diodes as part of module design to ensure satisfactory "hot-spot" performance. Under those circumstances, the internal mounting approach pictured in Figure 1(c) is preferred over the externally-mounted implementation shown in Figure 1(e) since the latter approach would require the repeated penetration of the module encapsulant for connections to the externally-mounted diodes.

The motives of the array designer are somewhat broader since the measure of success in this area is the maximization of array energy output over the operational lifetime of the installation in the face of shadowing and various internal module failures as well as the avoidance of system level fire and personnel safety problems. Again, when properly installed, bypass diodes can aid in the achievement of these array design objectives.

Beginning with a module which follows the recommended bypass diode application guidelines discussed above (i.e., a configuration with no diodes or with multiple internal diodes), Figure 2(a) illustrates the options available to an array designer in a circuit arrangement consisting of a parallel-connection of series strings. An implementation that uses no bypass diodes in the array circuit is not considered to be an appropriate solution when the objectives of the array design can be better achieved by one of the other arrangements shown. If the module contains no integral bypass diodes, the array designer should install a diode around each series-connected circuit element as shown. However, if the selected module design contains multiple internal diodes, it may be adequate to simply series-connect these modules with no additional diodes. It may also be appropriate for the array designer to add bypass diodes in parallel with the existing internal module diodes as shown on the right hand side of Figure 2(a). Such an arrangement can function to eliminate arcing upon module removal if the array-installed diodes are wired to maintain circuit continuity through the interconnecting harness.

For an arrangement of series-connected parallel groups, one bypass diode can be employed for each of the groups as illustrated in the bottom half of Figure 2(b). This array-installed diode must have the forward current rating and power dissipation capability necessary to accommodate the accumulative short-circuit current output from the parallel-connected modules within the group. For the case where the modules are equipped with multiple internal diodes, the installation of one large diode per group assures that the bypass current will pass through the external circuit, thus avoiding the problems associated with current sharing among the internal diodes if no such external diodes were present.

As an outcome of this reasoning, the array designer is left with the five acceptable diode electrical integration options illustrated in Figure 2. It is appropriate at this point to make some general observations regarding the applicability of these acceptable options to arrays of various power and voltage levels. Moderate voltage (100 to 200 vdc) and moderate power (1 to 5 kw) arrays, which have a wide applicability to roof-mounted residential systems, can generally be characterized as having a relatively high voltage module since the driving requirement is to develop the required inverter input voltage level within the limited roof area available. Since the desire to maximize the module size within the constraints imposed by the roof installation will also limit the number of modules in the array, these systems will generally be configured as parallel-connected series strings where each
string represents a source circuit. In such a system, the selection from among the acceptable bypass diode integration options in Figure 2(a) will depend on the bypass diode implementation approach adopted by the module designer. If the module voltage is sufficiently low or if the cell reverse voltage characteristics are sufficiently soft, the module may not be configured with integral diodes, leaving the array designer with the requirement to install a bypass diode around each module in each source circuit. If the module voltage is high enough to require the use of multiple integral bypass diodes, it may suffice to simply series-connect these modules to form a source circuit with no additional bypass diode protection. However, such an interconnection will require individual source circuit interrupts to avoid arcing when a module is removed from an illuminated array. The addition of external bypass diodes, which are connected in parallel with the internal module diodes on the harness side of the module connect means, will eliminate this potential for arcing.

As the array voltage level and power output increase, the array interconnection scheme will be driven toward an approach using a series connection of parallel groups as shown in Figure 2(b). The modules used for such high voltage/high power applications will generally be characterized as large in physical size with a relatively low output voltage. These two attributes will tend to minimize the number of source circuits in the array field, but for central station applications where the output power exceeds 1 MW peak, it will probably still be necessary to combine modules into parallel groups within each source circuit to further limit the number of source circuits. The number of modules of a particular design in each of these parallel groups will depend on system level cost considerations which include the effects of field wiring and fault protection and isolation. For high power array field installations, it would not be unreasonable to expect the individual source circuit current to exceed 60 amperes. In these cases, the single bypass diode servicing each parallel group of modules must be sized and mounted to dissipate the heat generated by this level of source circuit current.

**BYPASS DIODE IMPLEMENTATION OPTIONS**

Conventional packaging approaches involve the mounting of a standard diode configuration within an enclosure with a suitably-sized heat sink. The approaches described below have the potential for lower cost through the reduction of the thermal resistance between the diode junction and the ambient air with the associated reduction in the required heat sink surface area and through the elimination of ancillary components required for electrical isolation and environmental protection. The unique feature of these designs involves the direct use of a mounted diode cell as opposed to a conventional packaged diode. The advantages of such an implementation include: (1) the lower thermal resistance associated with the elimination of mounting interfaces, some of which may be mechanical contact surfaces; (2) the reduction in the volume required for the diode package; and (3) the elimination of ancillary mounting hardware such as nuts, lockwashers, insulating washers and sleeves, and cathode terminals.

**Internally Encapsulated**

The lamination of a diode cell/heat spreader within the module encapsulant, as shown in Figure 3, was the first such implementation considered. This packaging approach solves many of the problems inherent in an externally-mounted package, including: (1) the location of a suitable mounting area which is large enough to accommodate the external enclosure with its associated heat sink, (2) the electrical bonding of the metallic heat sink to the module or array structural ground, and (3) the isolation of the electrically active parts of the diode assembly from contact by personnel.

![Figure 3. Typical Glass Superstrate Lamination Stack-up with Encapsulated Bypass Diode](image)

The dissipation of the heat generated within the small diode chip when conducting the bypass current represents the most difficult design problem involved with the integration of these chips within the module encapsulant. It is also essential that the thickness of the package to be laminated along with the solar cell circuit be kept as small as possible to maintain conformance of the rear cover sheet with the minimum use of encapsulant material. These requirements combine to dictate that the diode chip be mounted to a thin heat spreader plate which is fabricated from a material of high thermal conductivity. In this way, it is possible to maintain an acceptably low junction temperature by transferring the heat from this small source through the fin created by the plate and on out into the adjacent solar cell circuit elements where it can be ultimately rejected to the surroundings by radiation and convection. The size of the heat spreader plate required to produce the specified temperature level within the laminate will depend on the diode heat generation as well as on the insolation level, ambient temperature, wind speed and details of the module mounting...
In Figure 5, again, as in the encapsulated diode case, the packaging approach centers around the mounting of a diode cell to a heat spreader, but in this instance, the heat spreader is a beryllia disk which also functions as the electrical insulator between the diode cathode terminal and the grounded aluminum heat sink cover (2). The diode cell is soldered directly to a metallization pattern on the beryllia disk. The other side of this disk is coated with thermal grease and located within a spotfaced area on the finned heat sink cover where it is pressed against the cover by a pair of leaf springs which also serve as the anode and cathode contacts for the diode. With this diode mounting method, it is possible to achieve an extremely low value for the thermal resistance between the diode junction and the heat sink. This parameter, which is identified as $R_{jgs}$ in Figure 6, has a direct influence

\[ Q = \frac{J_{sc} R_{jgs}}{T_{j} - T_{a}} \]

Figure 6. Thermal Path Between the Diode Junction and Ambient

<table>
<thead>
<tr>
<th>$Q$</th>
<th>Diode Heat Dissipation</th>
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</thead>
<tbody>
<tr>
<td>$R_{jgs}$</td>
<td>Diode Junction Temperature ($T_j$)</td>
</tr>
<tr>
<td>$R_{gs}$</td>
<td>Heat Sink Temperature ($T_s$)</td>
</tr>
<tr>
<td>$R_{gsa}$</td>
<td>Ambient Air Temperature ($T_a$)</td>
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</table>

The encapsulation of bypass diodes within a module laminate is a particularly attractive solution when it is necessary, because of "hot-spot" heating considerations, to provide multiple bypass diodes within a module. Under this condition, the internally-encapsulated packaging can provide the required bypass diode protection without intermediate penetrations of the encapsulant which would otherwise be necessary to connect the externally-mounted diodes to solar cell circuit tap points.

Externally Mounted

Under other conditions, where the array designer requires a bypass diode around each series-connected module within a source circuit, it might be advantageous to consider the integration of the diode function with the module electrical terminations and wiring harness connect means. One such implementation approach, which was found to have the lowest cost of the concepts considered, is illustrated...
on the heat sink required to limit the diode junction temperature during worst-case ambient temperature conditions. Using the nomenclature defined in Figure 6, the heat dissipation capability of the mounted disk, Q, is given by:

\[
Q = \frac{T_i - T_a}{R_{\text{eqj}} + R_{\text{esa}}}
\]

The heat transfer through the stacked assembly of diode cell and beryllia disk can be modelled using the method outlined in Reference (3) to yield the thermal resistance values shown in Figure 7 as a function of the physical parameters including die diameter (d), BeO disk diameter (D) and thickness (tB). These data reveal the importance of the BeO disk in spreading the heat flow path so that the area of the grease interface is effectively increased, resulting in its reduced impact on the overall thermal resistance of the stack-up.

![Figure 7. Thermal Resistance of the Diode Cell/Beryllia Disk Assembly](image)

The selection of silicon die size and BeO wafer diameter and thickness cannot be made independent of a consideration of heat sink size since the former parameters determine the \(R_{\text{eqj}}\) value while the heat sink size is directly related to the \(R_{\text{esa}}\) value. As shown in Figure 6, it is the sum of these two thermal resistance values that determines the ability of the assembly to achieve a given junction temperature rise under a specified heat dissipation condition. As the silicon die and BeO disk are reduced in size to minimize the cost of these components, the corresponding \(R_{\text{eqj}}\) value will increase forcing a commensurate decrease in the required \(R_{\text{esa}}\) value. This decrease in \(R_{\text{esa}}\) requires a correspondingly larger heat sink with associated higher cost. Conversely, the specification of an undersized heat sink will force a corresponding lower value of \(R_{\text{eqj}}\) which can only be achieved by specifying a larger silicon die and/or BeO wafer size.

**RELIABILITY CONSIDERATIONS**

Photovoltaic module bypass diodes operate in a manner which is characterized by the periodic application of a relatively low reverse voltage. This reverse voltage will generally be less than 15 Vdc and will be applied as 12 hours "ON" followed by 12 hours "OFF". Since there will be negligible diode power dissipation during this period, the diode temperature will approximate the solar cell temperature. This temperature will approach the ambient temperature during nighttime or "OFF" periods and will be elevated above the ambient temperature during daylight periods by an amount which varies with the solar intensity and wind speed and direction. Occasionally, the bypass diodes may be required to conduct current in the forward direction at a level which varies with insolation level and circuit loading conditions.

The predominant failure mechanisms found in semiconductor services are related to junction temperature and fit the Arrhenius model as shown in Figure 8 for a typical rectifying diode.

![Figure 8. Failure Rate for a Typical Rectifying Diode](image)
The criteria for failure pertain to the rectifying application and generally include a low threshold of leakage current (10 to 500 μA) at a specified reverse voltage as well as a small change in the forward voltage drop (10 to 100 mV) at a specified forward current. No failure rate data is available for the operation of power diodes in the continuous dc reverse voltage blocking mode which is typical of the normal bypass diode operating condition. There is a general agreement among experts in this field that the continuous dc reverse voltage operation will tend to increase the leakage current with time compared to a normal ac rectifying application. However, the failure limit for reverse voltage leakage current in a photovoltaic module bypass application can be many orders of magnitude higher than that for the power rectifier and still operate satisfactorily.

Notwithstanding the obvious shortcomings in the available failure rate data as it might be applicable to the bypass diode operating conditions, it is possible to draw certain conclusions based upon rectifying diode data. For the photovoltaic module bypass application, the diode reliability will be almost exclusively determined by the bias operating conditions since the exposure time under these conditions is many orders of magnitude larger than the expected exposure to a forward conducting operating condition. Fortunately, the average junction temperature under these reverse bias operating conditions is relatively low, with 45°C being the maximum expected average temperature for a U.S. site location. Also, the magnitude of the reverse voltage is a small fraction of the lowest available rated value for PN junction devices. These two factors combine to yield a low failure rate for this diode application based on the available data.

CONCLUSIONS

If the module design dictates multiple bypass diodes, the responsible designer should use the internally encapsulated packaging approach to avoid the intermediate penetrations of the laminate that would otherwise occur. The integration of bypass diodes at the array design level will entail the external mounting of these devices using a method that is tailored to the required current carrying capacity of the installation and the desired source circuit wiring configuration. For an array circuit layout consisting of a parallel connection of series strings, the array designer should package the bypass diode in a module-mounted enclosure which is integral with the module connect means. Unpackaged PN junction diode cells mounted to beryllia heat spreaders can be employed within these enclosures to reduce the overall thermal resistance of the installation so that bypass currents of up to 30 amperes can be accommodated with a heat sink size which is compatible with the module-mounted installation. For a source circuit that is configured as a series connection of parallel groups of modules, the array designer should use a single diode for each parallel group to avoid the problems associated with diode current sharing. Since the current handling capability of this installation will generally be larger than the previous circuit arrangement, the required heat sink and enclosure should be mounted to an appropriately sized structural member on the array panel. The current handling capability of such an installation will be limited by heat rejection considerations under worst case ambient conditions including a high air temperature with zero wind speed. Thus, for a given specification of those ambient conditions, there is a practical upper limit on the ampacity of an individual bypass diode installation which is dictated by the ability to limit the diode junction temperature to an acceptable level without requiring ancillary forced air or liquid cooling.

REFERENCES